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APPLICATION OF SILICON PIEZORESISTIVE STRESS TEST CHIPS IN ELECTRONIC PACKAGES

Yida Zou

A Dissertation

Submitted to

The Graduate Faculty of

Auburn University

In Partial Fulfillment of the

Degree of

Doctor of Philosophy

Auburn, Alabama

August 30, 1999

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APPLICATION OF SILICON PIEZORESISTIVE STRESS TEST CHIPS IN ELECTRONIC PACKAGES

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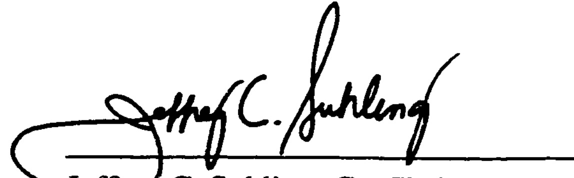

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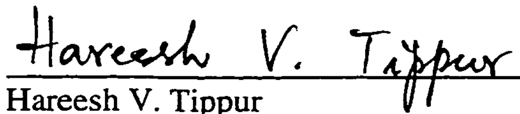

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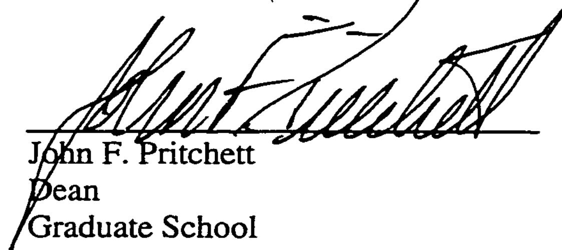

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DISSERTATION ABSTRACT

APPLICATION OF SILICON PIEZORESISTIVE STRESS TEST CHIPS IN ELECTRONIC PACKAGES

Yida Zou

Doctor of Philosophy, August 30, 1999
(M. S., East China Institute of Technology, 1991)
(B. S., East China Institute of Technology, 1988)

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Directed by Jeffrey C. Suhling and Richard C. Jaeger

In this work, both special (100) and (111) silicon test chips containing an array of optimized piezoresistive stress sensor rosettes have been successfully applied within several electronic packaging configurations. Unlike (100) silicon test chips, (111) silicon test chips are able to measure the complete stress state on the die surface. After calibration and characterization of the test chips, they were packaged into various assemblies. The post packaging resistances of the sensors were then recorded at room temperature, as a function of temperature excursion, and during long term packaging reliability qualification tests (thermal cycling and thermal aging). The stresses on the die surface were calculated using the measured resistance changes and the appropriate theoretical equations. For comparison purposes, three-dimensional nonlinear finite element simulations of the

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packaging processes were also performed, and the stress predictions were correlated with the experimental test chip data.

AAA2 (100) silicon test chips containing optimized four element dual polarity rosettes have been applied within 44 pin Plastic Leaded Chip Carrier (PLCC) packages and 240 pin Quad Flat Packs (QFP's). In these plastic package experiments, comparison of the stress levels induced by various molding compounds was emphasized. Advanced (111) silicon test chips (BMW-1 or BMW-2) comprising an array of optimized eight-element dual polarity piezoresistive sensor rosettes were encapsulated in 240 pin QFP's, 160 pin QFP's, Chip on Board (COB) packages, and 281 pin ceramic Pin Grid Array (PGA) packages. In addition to molding compound evaluations, BMW-1 test chips encapsulated in 240 pin QFP's were used to detect the presence of delaminations between the die surface and the encapsulant. In the wire bonded COB package studies, die surface stress evaluations were conducted after die attachment, and throughout the cure cycle of the liquid encapsulant. The stresses were also studied as a function of temperature, and then measured during reliability testing (thermal cycling and high humidity storage). Furthermore, a comparison of COB stress levels obtained with convection and variable frequency microwave encapsulant curing was performed. Finally, stress levels were evaluated within 281 pin ceramic PGA packages using high temperature die-attachment materials. Variations in the package stress levels were monitored during thermal cycling and thermal aging reliability tests.

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CHAPTER 1

INTRODUCTION

Stresses due to thermal and mechanical loadings are often produced in chips which are incorporated into electronic packages. During fabrication steps such as encapsulation and die attachment, thermally-induced stresses are created. These occur due to non-uniform thermal expansions resulting from mismatches between the coefficients of thermal expansion of the materials comprising the package and the semiconductor die. Additional thermally-induced stresses can be produced from heat dissipated by high power density devices during operation. Finally, mechanical loading can be transmitted to the package through contact with the printed circuit board to which it is mounted. The combination of all of the above loadings can lead to two-dimensional (biaxial) and three-dimensional (triaxial) states of stress on the surface of the die. If high-power density devices within the package are switched on and off, these stress states can be cyclic in time causing fatigue loading. All of these factors can lead to premature failure of the package such as fracture of the die, severing of bond connections, die attach failure, and encapsulant cracking. These reliability problems are of ever increasing concern as larger scale chips and higher temperature applications are considered.

Stress analyses of electronic packages and their components have been performed using analytical, numerical, and experimental methods. Analytical investigations have been primarily concerned with finding closed-form elasticity solutions for layered

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structures, while numerical studies have typically considered finite element solutions for sophisticated package geometries. Experimental approaches have included the use of test chips incorporating piezoresistive stress sensors (semiconductor strain gages), and the use of optical techniques such as holographic interferometry, moiré interferometry, and photoelasticity.

Piezoresistive stress sensors are a powerful tool for experimental structural analysis of electronic packages. Figure 1 illustrates the basic application concepts. The structures of interest are semiconductor (e. g. silicon) chips which are incorporated into electronic packages. The sensors are resistors which are conveniently fabricated into the surface of the die using current microelectronic technology. The sensors are <u>not</u> mounted on the chips. Rather, they are an integral part of the structure (chip) to be analyzed by the way of the fabrication process. The stresses in the chip produce resistance changes in the sensors (due to the piezoresistive effect) that can be measured. Therefore, the sensors are capable of providing non-intrusive measurements of surface stress states on a chip even within encapsulated packages (where they are embedded sensors). If the piezoresistive sensors are calibrated over a wide temperature range, thermally-induced stresses can be measured. Finally, a full-field mapping of the stress distribution over the surface of a die can be obtained using specially designed test chips which incorporate an array of sensor rosettes.

Prior publications on stress sensing test chips have included sensor rosettes with up to eight resistors. Using n-type and p-type sensors at various orientations, several or all the stress components on the die surface can be measured. By monitoring packaging stresses using stress sensing test chips, a variety of accomplishments have been achieved. For instance, test chips have been used to provide a better understanding of the shear stress

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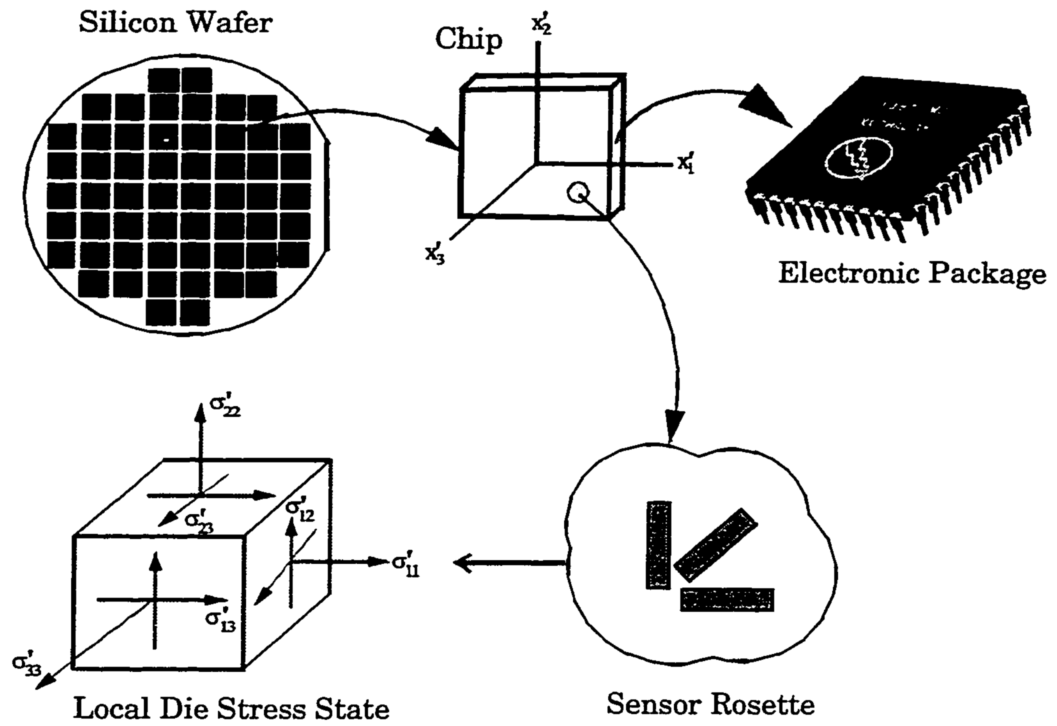

Figure 1.1 – Piezoresistive Sensor Concept

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failure mechanisms in plastic packages. In addition, thermal stresses due to die attachment, molding, and temperature variation have been characterized. The effects of die size and package configuration on the stresses after molding have also been quantified for various package pin counts. Piezoresistive measurements have allowed molding compound materials to be evaluated with respect to their thermal-induced stress levels. Also, the effects of thermal cycling and delamination at the chip/encapsulant interface can be explored using test chips. Recently, thermal stress measurements of epoxy underfilled flip-chip on board devices were reported, and the effects of the curing conditions of the underfills were investigated.

Theoretical analysis has established that properly designed sensor rosettes on the (111) silicon wafer plane have several advantages relative to sensors fabricated using standard (100) silicon. In particular, optimized rosettes on (111) silicon can be used to measure the complete state of stress (six stress components) at a point on the top surface of the die, while optimized rosettes on (100) silicon can measure at most four stress components. Also, optimized sensors on (111) silicon offer the unique capability of measuring four temperature compensated combined stress components, while those on (100) silicon can only be used to measure two temperature compensated quantities. Furthermore, it has been established that the (111) plane offers the opportunity to measure the highest number of stress components in a temperature compensated manner. This is particularly important, given the large thermally induced errors which can often be found in stress sensor data. The four stress components which can be measured in a temperature compensated manner using (111) silicon sensors are the three shear stress components and the difference of the in-plane normal stress components.

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In this work, (100) and (111) silicon test chips containing an array of optimized piezoresistive stress sensor rosettes, which were designed and fabricated in Auburn University, have been successfully applied within several electronic packaging configurations. Calibrated and characterized stress test chips were assembled into various packaging configurations. The post packaging resistances of the sensors were then recorded. These packaging resistances were monitored at room temperature, as a function of temperature excursion, or during long term packaging reliability qualification tests (thermal cycling and thermal aging). The stresses on the die surface were calculated using the measured resistance changes and the appropriate theoretical equations. For comparison purpose, three-dimensional nonlinear finite element simulations of the plastic encapsulated packages were also performed, and the stress predictions were correlated with the experimental test chip data.

Silicon piezoresistive theory has been reviewed to allow for understanding of the equations utilized for stress calculation on the die surface. General resistance change equations were expressed in the unprimed crystallographic system, and in an arbitrarily rotated primed coordinate system. The ensuing resistance change equations for (100) and (111) silicon wafer planes were then extracted. The (100) silicon test chip (AAA-2) utilized in this work incorporates an array of optimized four-element dual polarity sensor rosettes for stress measurements. Each of these rosettes contains a 0-90° p-type resistor pair and a $\pm 45^{o}$ n-type resistor pair. It has been demonstrated that this choice of sensor orientations minimizes thermally induced errors as well as those due to resistor misalignment, maximizes stress sensitivity, and permits accurate temperature compensated measurement of the values of in-plane normal stress difference $(\sigma'_{11} - \sigma'_{22})$ and the in-plane

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shear stress σ'_{12}. The (111) silicon test chips (BMW-1 or BMW-2) used in this study contain p-type and n-type sensor sets, each with resistor elements making angles of $\Phi = 0$, ± 45, 90° with respect to x'_1-axis perpendicular to the wafer flat. This eight-element dual polarity rosette has been optimized to measure all six stress components (four in a temperature compensated manner). This is a particularly important attribute, given the large errors which can be introduced into non-temperature compensated stress sensor data when the temperature change T is not precisely known. The four measurable temperature compensated stress components are $(\sigma'_{11} - \sigma'_{22})$, σ'_{12}, σ'_{13}, σ'_{23}.

The AAA-2 (100) silicon test chips containing optimized four-element dual polarity rosettes have been applied within plastic electronic packaging configurations including 44 pin Plastic Leaded Chip Carrier (PLCC) packages and 240 pin Quad Flat Packs (QFP's). In the PLCC stress studies, 100 x 100 mil test chips were encapsulated. Several molding compounds were considered and the stress levels were compared. Larger 450 x 450 mil AAA-2 test chips were used in 240 pin QFP's. No delaminations between the die surface and encapsulant occurred, and these measurement results then served as a reference for subsequent stress evaluations within delaminated QFP's. For all the packaging configurations, three-dimensional nonlinear finite element simulations were performed to correlate with the experimental results.

Advanced (111) silicon test chips (BMW-1 or BMW-2) comprising an array of optimized eight-element dual polarity piezoresistive sensor rosettes played a key role in recent stress assessments. Chips with dimensions of 400 x 400 mils were encapsulated in 240 pin QFP's, 160 pin QFP's, Chip on Board (COB) packages, and 281 pin ceramic Pin

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Grid Array (PGA) packages. BMW-1 and BMW-2 test chips were used to characterize 240 pin QFP's, and the presence and extent of delaminations between the die surface and the encapsulant was explored using C-Mode Scanning Acoustic Microscopy (C-SAM). The stress distributions in delaminated packages were then compared with those in non-delaminated packages. Two different molding compounds were used in the stress measurements within 160 pin QFP's. The post molded room temperature stress results were then compared.

Die stresses in wire bonded COB packages were measured using BMW-2 silicon stress test chips encapsulated in two molding compounds. The stress sensing rosettes were characterized after die attachment, and throughout the cure cycle of the liquid encapsulant. Using the measured data and appropriate theoretical equations, the stresses at sites on the die surface have been calculated. Also, the packaged die stresses were studied as a function of temperature. After these investigations, additional COB package studies were performed. In this case, a comparison of COB stress levels with convection and variable frequency microwave encapsulant curing was carried out. Stress comparisons were made throughout the entire packaging processes. Thermal cycling and high humidity storage reliability tests were conducted on some of the COB samples. The stress variations were studied as a function of the number of thermal cycles, and with the duration of moisture absorption. The comparison of stress shifts occurring with the two encapsulant curing methods was then made.

High temperature die-attachment materials were evaluated by applying BMW2 test chips within 281 pin ceramic PGA packages. Six adhesives were utilized in these experiments including silver filled glasses, polyimide pastes, thermoplastic films, and gold

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germanium. A comparison of die stresses at room temperature caused by the different die attachment materials has been made. The stresses on the die surface were also extracted as a function of temperature when a single thermal cycle was applied. In addition, thermal aging and thermal cycling tests were conducted on the PGA packages. The die attachment materials were evaluated by the stress changes occurring during these reliability tests.

Finally, nonlinear finite element simulations of the 240 pin QFP, 160 pin QFP, COB, and 281 pin ceramic PGA packages were performed, and the predicted die stresses were correlated with the test chip measurements. Anisotropic (111) silicon material properties were used, while isotropic properties were assumed for materials other than silicon die. The materials were modeled as linear elastic with temperature dependent properties, and large deformations (kinematic nonlinearities) were utilized.

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CHAPTER 2

LITERATURE REVIEW

Mechanical stresses are typically built into silicon device structures at virtually every stage of manufacture. Dale and Oldfield [1] addressed stress generation in packaging processes such as wafer preparation, oxidation, diffusion, metallization, die and wire bonding, encapsulation, and curing. Lau [2] has discussed several problems associated with stress, including package cracking, wire damage, and thin film cracking on the die. Stress generation mechanisms were also discussed with respect to die attachment, encapsulation, surface mounting processes, and bending during application. Nguyen [3] has presented current reliability issues involved with typical postmold IC packages. One of the four major concerns is stress. Issues such as stress mechanisms and measurement were reviewed.

The trend towards high integration of circuits has given rise to rapidly increasing stress fields in plastic packages because of the mismatches of the thermal expansion coefficients of dissimilar packaging materials. Mechanical and electrical failures due to induced thermal stresses have been documented since the 1970's. Within a plastic package, out-of-plane shear stresses act on the chip surface with the traction direction toward the center of the chip, causing deformation of the die metallization. With chips coated with passivation glass, these deformations can cause passivation cracking.

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Microcracks in the plastic encapsulant or delamination at the die-encapsulant interface promote metal deformation, since they reduce the restrictions on plastic movement at the chip surface [4-8]. Isagawa, et al. [4] observed the deformation of aluminum metallization during thermal shock tests of plastic packages. The deformations were related to encapsulant properties, chip size, test temperature range, etc. Thomas [5] performed thermal cycling on molded packages containing unpassivated test chips. Lundström and Gustafsson [6], Lesk, et al. [7], and Edwards, et al. [8] also described metal shift or damage during thermal shock or thermal cycling tests.

Shear stresses are heavily concentrated at the corners and edges of the silicon die, and can result in thin film brittle passivation cracking or interlayer dielectric film cracking [9-15]. Okikawa, et al. [9-10] and Shirley, et al. [11] presented studies of thin film cracks due to thermal stresses. Foehringer, et al. [12] described a model which explained the interactions among the key variables related to thin film cracking. The effort to model the failure rate as a function of environmental stress severity was done by Blish and Vaney [13]. A special test chip was designed by Gee, et al. [14] to detect thin film cracking in PLCC packages with various pin counts, die sizes, thermal cycling numbers, etc. Inayoshi [15] demonstrated that stresses can disrupt the chip passivation, permitting moisture to penetrate through to the underlying aluminum metallization causing corrosion.

Delamination at the chip-encapsulant interface is believed to be the result of critical shear stresses on the die surface, and usually occurs during reliability tests, such as temperature cycling and Highly Accelerated Stress Testing (HAST). The

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delaminations typically start at the corners of the silicon die, and proceed toward the chip center [16-23]. Nishimura, et al. [16] confirmed the delamination at the die-encapsulant interface using ultrasonic inspection techniques. Doorselaer, et al. [17] revealed the relation between electrical failures and delamination. Moore, et al. [18-20] applied C-SAM (C-Mode Scanning Acoustic Microscopy) technique to inspect delaminations and cracks in IC packages. The evaluations were performed with various molding compounds, lead frame finishes, and die surface conditions. A comparison of delamination effects between temperature cycling and HAST tests was carried out by van Gestel, et al. [21-22]. Delaminations at the chip-encapsulant interface of 240 pin QFP packages were also found by Zou, et al. [23] even before reliability tests. Interfacial adhesion is one of the key factors to achieve delamination free packaging. Evaluations of various interfaces in plastic packages were conducted by Nguyen, et al. [24-26].

The occurrence of microcracks in the encapsulant is another serious reliability issue with plastic packages. The microcracks usually initiate at the chip edges, then propagate into the encapsulant at roughly a 135° angle from the chip surface [5]. Thermal cycling between -55°C and 150°C was performed on Dual Inline Packages by Nishimura, et al. [16, 27]. Package cracking was observed as a function of the number of temperature cycles for different encapsulant and lead frame materials. The presence of microcracks in the encapsulant dramatically changes the stress distribution in a package. A tentative model was proposed by Schroen, et al. [28] to describe the stress relief and oscillation measurements during temperature cycling tests. The stresses causing the cracks are so high that may cut through silica filler particles [7]. To avoid high stress,

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suggestions such as development of plastic encapsulants with low CTE, low elasticity modulus, high strength, optimized plastic curing processes, and prevention of moisture absorption, have been proposed or practiced [28-31].

Large residual stresses introduced during packaging procedures, especially die attachment and encapsulation steps, can also cause die cracks. Since silicon is an extremely brittle material, minor surface flaws can act as crack starters in the presence of tensile stresses [32, 33]. Improper dicing of silicon wafers is another contributor to die cracking [1].

Electronic characteristic changes occur in IC chips due to mechanical stresses introduced by packaging processes. The resistivity of diffused resistors shifts due to piezoresistive effects, so that piezoresistive stress sensors can be developed [34-36]. Other device characteristics shifts were also experimentally studied, or observed in actual plastic packaged devices [37-45]. Using the relations between MOS drain current change and the acting stresses, stress sensors based on piezoresistive field effect transistors (PIFET's) were proposed and designed [43-45].

To understand the stress developed in plastic packages during packaging processes, reliability tests, and actual applications, researchers have performed stress analyses using analytical, numerical, and experimental methodologies.

Suhir [46-49] and Liew, et al. [50] suggested analytical methods for evaluation of the interfacial stresses in bimetal thermostats based on elementary beam (or long-and-narrow plate) theory. Tay, et al. [51-53] discussed the mechanics of interfacial delamination, and presented analytical methods to describe moisture-induced

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delamination growth during solder reflow. These analytical models were correlated with experimental observations to help understand failure mechanisms.

Finite element simulations provide useful insight into the stress distributions produced in plastic packages during die attachment, encapsulation, and reliability tests. Various package configurations, packaging material combinations, and conditions related to package processes and reliability tests can be investigated by means of finite element methods [54-67]. In early finite element modeling, Groothuis, et al. [54] and Pendse [55] displayed the effects of material choices and structure changes on stress variation within a DIP package. Kelly, et al. [56-59] demonstrated how thermal stresses are developed within a plastic package, and suggested innovations in processes such as a side buffer of soft material, etc. Mertol [60] studied the thermal stresses in a high pin count PQFPs.

In two-dimensional finite element simulations of plastic packages, plane strain analyses would be more suitable for prismatic bodies (DIPs and SOPs), while packages with square features (PLCC, PQFP) could be represented by coaxial rings using axisymetric analyses [3]. van Gestel, et al. [61] used three layers of special interface elements to simulate delamination behavior when plastic packages were subjected thermal cycling. Sweet, et al. [62], applied a linear viscoelastic model to predict die surface stresses. Effects of various delamination conditions to die surface stress distributions were also evaluated. Liu, et al. [63-64] built finite element models to predict thermal deformation and delamination in PQFP's and made comparison with moiré interferometry testing data. Yeung, et al. [65] and Park, et al. [66] used finite

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element analysis to evaluate the thermal residual stress in a PQFP assuming viscoelastic stress-strain behavior of the molding compounds.

Analytical solutions are difficult to achieve for complex packaging configurations. Although the finite element method (FEM) is a reliable modeling tool to predict stress distributions within packages, the computational results have to be verified by experimental analysis. In addition, finite element simulations are limited by the availability of packaging material properties, accurate understanding of packaging processes, and other assumptions and approximations. Thus, it is desirable to develop experimental stress analysis methods for electronic packages. Moiré interferometry was applied by Bastawros, et al. [67], Han and Guo [68], and Liu, et al. [63-64] to measure thermal deformations within packages. Shadow Moiré methods were effective in evaluating the warpage of packages [69-70]. Some other testing and measurement techniques were reviewed by Guo and Sarihan [71].

The piezoresistive effect is caused by the change of resistivity of semiconductors as a function of applied stresses. Smith [72] first proposed to use the piezoresistive behavior of semiconductors for stress and strain measurements. Since then, Tufte and Stezer [73] and Suhling, et al. [74-75] have investigated the temperature dependence of piezoresistive coefficients of silicon or germanium. Kanda [76] represented the piezoresistive coefficients graphically. Yamada, et al. [77] addressed the nonlinearity of the piezoresistive effect. Dally and Riley [78] discussed the properties and performance characteristics of semiconductor strain gauges. The detailed theory for silicon

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piezoresistive sensors was derived by Bittle, et al. [35, 79], and Kang [80] developed piezoresistive theory for silicon on various wafer planes and for silicon carbide.

Piezoresistive sensors are a powerful tool for experimental structural analysis of electronic packages. The sensors are resistors which are conveniently fabricated into the surface of the die using current microelectronic technology, and are capable of providing non-intrusive measurements of surface stress state on a chip even within encapsulated packages [81-82].

Several investigators have used stress test chips based on piezoresistive sensors to examine die stresses in plastic encapsulated packages. In early studies, Edwards and co-workers [8, 28, 83-84], Groothuis, et al. [54], and van Kessel, et al. [32] used (100) silicon test chips based on 0-90 two-element sensor rosettes to examine stresses in small pin count packages. Resistance changes of sensors during thermal cycling and pressure cooker environment tests were compared [28]. Die stress studies were utilized to direct the selection of packaging materials and the control of packaging processes [83-84]. The mechanism of structure failures were also investigated [32, 42, 54].

Gee and co-workers [85-87] have mapped die surface stress distributions using (111) test chips containing an array of four element 0-±45-90° sensor rosettes. In these studies, tests were also performed to understand the effects of package geometrical parameters and thermal cycling on the die stress levels. Further investigations with these chips were performed on 40 pin dual in-line packages (DIP's) by van Gestel and co-workers [88-89]. In addition, Lead frames and molding compounds were studied by Lundström, et al. [6] using a (111) silicon test chip with p-type four-element rosettes.

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Temperature dependent stress state measurements after die attachment and encapsulation were examined by Natarajan, et al. using n-type (100) silicon test chips [90].

Miura, et al. [91-94, 36, 39] have used (100) test chips incorporating four-element dual-polarity rosettes (0-90° n-type resistors and ±45° p-type resistors) to characterize thermally-induced die stresses in DIP's. Their sensor rosette design was the first capable of measuring the out-of-plane normal stress perpendicular to the die surface. In one of these studies, the effects of internal structure on plastic packaging reliability were explored [93]. The level of die stress was studied as a function of temperature changes and thermal cycling tests [36]. Delamination at the interface of die/encapsulant was also correlated to varied stress magnitudes [39]. Zou, et al. [95] have recently used (100) test chips based on a similar rosette with reversed doping polarities (0-90° p-type resistors and ±45° n-type resistors) to characterize the stresses in plastic leaded chip carrier (PLCC) packages that were encapsulated using several different molding compounds. Sweet and co-workers [34, 62, 96-98] have used the (100) silicon Sandia ATC-04 test chip to investigate liquid encapsulation of integrated circuit die mounted directly on ceramic substrates, and to study 160 pin quad flat packs (QFP's). The ATC-04 contains a multiplexed array of sensor rosettes. Each dual-polarity rosette contains eight resistors (0-±45°-90° orientations for both p-type and n-type resistors).

Other experimental studies using test chips with piezoresistive stress sensors can be found in the literature [99-109]. Skipor, et al. [99] compared both stress measurements using test chips and displacement measurements using moiré interferometry with FEM calculations for 64 pin TQFP and 68 pin PLCC packages. Lo,

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et al. [100-101] and Bossche, et al. [102-103] described the design, fabrication, and calibration of their own stress test chips. Ducos, et al. [104] presented the in-situ stress measurements during package assembly. Nysaether, et al. [105-106] examined the thermally-induced stresses in glob-on-top pressure sensor samples. Rey, et al. [107] associated creep of the solder joints in leaded components with stress measurements in the silicon die. They used experimental data together with the FEM simulations to find a mathematical model for creep in the solder. Palmer, et al. [108] attempted to measure the stress variation during plastic package molding. Sensor resistance measurements for test chips assembled into TBGA, MBGA, and ViperBGA™ packages were made by Thomas, et al. [109].

In recent applications of piezoresistive stress sensors, mechanical stresses in epoxy underfilled flip-chip on board packages were studied [110-114]. In-situ flip-chip assembly mechanical stress measurements using piezoresistive test chip were first reported by Peterson and co-workers [110]. In that work, die stresses were evaluated for several underfill materials. Nysæther, et al. [111] and Palaniappan, et al. [112] investigated the impact of curing parameters on the die stresses induced in flip-chip assembly processes. In reference [111], stress measurements were presented as a function of temperature when the underfill was cured at temperatures of 85 °C, 120 °C, and 150 °C. In reference [112], the residual die stresses were found to be strongly dependent on several underfill properties including CTE, storage modulus, T_g, and ultimately the underfill cure process. The effect of the choice of encapsulation material on the stresses during underfill cure, and preliminary stress measurements during thermal

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cycling were also reported by Palaniappan, et al. [113-114].

Theoretical analysis by Suhling and co-workers [35, 81-82, 115] has established that properly designed sensor rosettes on the (111) silicon wafer plane have several advantages relative to sensors fabricated using standard (100) silicon. Optimized rosettes on (111) silicon can be used to measure the complete state of stress (six stress components) at a point on the top surface of the die, and offer the unique capability of measuring four temperature compensated combined stress components. Suhling, et al. [81, 116] have used the (111) silicon BMW-1 test chip to make the first measurements of the complete state of stress (six stress components) on the surface of an encapsulated die. The BMW-1 chip incorporates dual-polarity eight element rosettes (0-±45°-90° orientations for both p-type and n-type resistors). In these studies, stresses were measured in chip on board (COB) packages where the test chips were bonded to FR-4 substrates and over-molded using "glob-top" liquid encapsulants. In addition to the in-plane stress components measured in the above studies, the first measurements of out-of-plane (interfacial) shear stresses at the die to encapsulant interface were recorded. The majority of the measurements were made at room temperature, but a demonstration of the variation of the die surface stresses with package temperature was also made. Results were correlated with the predictions of finite element simulations.

The (111) silicon BMW-1 test chip was also applied by Zou, et al. [23] to detect delaminations at the interface of the die and encapsulant. The stress distributions on the die surface in delaminated packages were compared with those in non-delaminated packages. The (111) silicon BMW-2 test chip was utilized by Zou, et al. [117-121] to

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characterize die surface stresses in various packaging configurations. The characterization of transient die stresses throughout the cure cycles of several chip-on-board (COB) encapsulants was performed [117-118]. High temperature die attachment adhesives were evaluated during thermal cycling and thermal aging tests in 281 pin Ceramic Pin Grid Array (CPGA) packages [119-120]. The comparison of die level stresses in COB packages processed with convection and variable frequency encapsulant curing were also made [121]. The experimental results were correlated to FEM simulations, and reasonable agreements were obtained [117-121]. Details of many of the above publications [23, 95, 117-121] are the subject of this dissertation.

Stress test chips need to be calibrated to obtain the piezoresistive coefficients required for the stress calculation. A four-point bending calibration procedure is typically used. Details of this method are discussed by Beaty, et al. [122], Bittle, et al. [35, 79], Suhling, et al. [74-75, 82], Jaeger, et al. [123-127] and van Gestal [89]. A wafer-level calibration technique was developed by Cordes [128] and Suhling, et al. [129-130]. A hydrostatic calibration method for (111) silicon test chips was developed and applied by Kang [80], and Suhling, et al. [82, 131].

An analysis of the errors associated with the design and calibration of piezoresistive stress sensors in (100) silicon has been made by Jaeger, et al. [132-133]. The significance of thermally induced errors in the calibration and application of silicon piezoresistive stress sensors was demonstrated by Jaeger, et al. [127]. A study on optimal temperature compensated piezoresistive stress sensor rosettes was presented by Suhling, et al. [115].

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CHAPTER 3

REVIEW OF PIEZORESISTIVITY THEORY

3.1 General Resistance Change Equations

An arbitrarily oriented silicon filamentary conductor is shown in Figure 3.1. The unprimed axes x_1 = [100], x_2 = [010], and x_3 = [001] are the principal crystallographic directions of the cubic (m3m) silicon crystal. The primed coordinate system is arbitrarily rotated with respect to this unprimed crystallographic system. For this conductor, the normalized change in resistance can be expressed in terms of the off-axis (primed) stress components using:

$$\frac{\Delta R}{R} = (\pi'_{1\alpha}\sigma'_\alpha)l'^2 + (\pi'_{2\alpha}\sigma'_\alpha)m'^2 + (\pi'_{3\alpha}\sigma'_\alpha)n'^2$$
$$+ 2(\pi'_{4\alpha}\sigma'_\alpha)l'n' + 2(\pi'_{5\alpha}\sigma'_\alpha)m'n' + 2(\pi'_{6\alpha}\sigma'_\alpha)l'm' \quad (3.1)$$
$$+ [\alpha_1 T + \alpha_2 T^2 + ...]$$

where $\pi'_{\alpha\beta}$ $(\alpha,\beta = 1, 2,..., 6)$ are the off-axis temperature dependent piezoresistive coefficients, $\alpha_1, \alpha_2, ...$ are the temperature coefficients of resistance, $T = T_m - T_{ref}$ is the difference between the measurement temperature and reference temperature (where the unstressed resistance R is measured), and l', m', n' are the direction cosines of the conductor orientation with respect to the x'_1, x'_2, x'_3 axes, respectively [35, 80, 81, 115,]. In Eq. (3.1)

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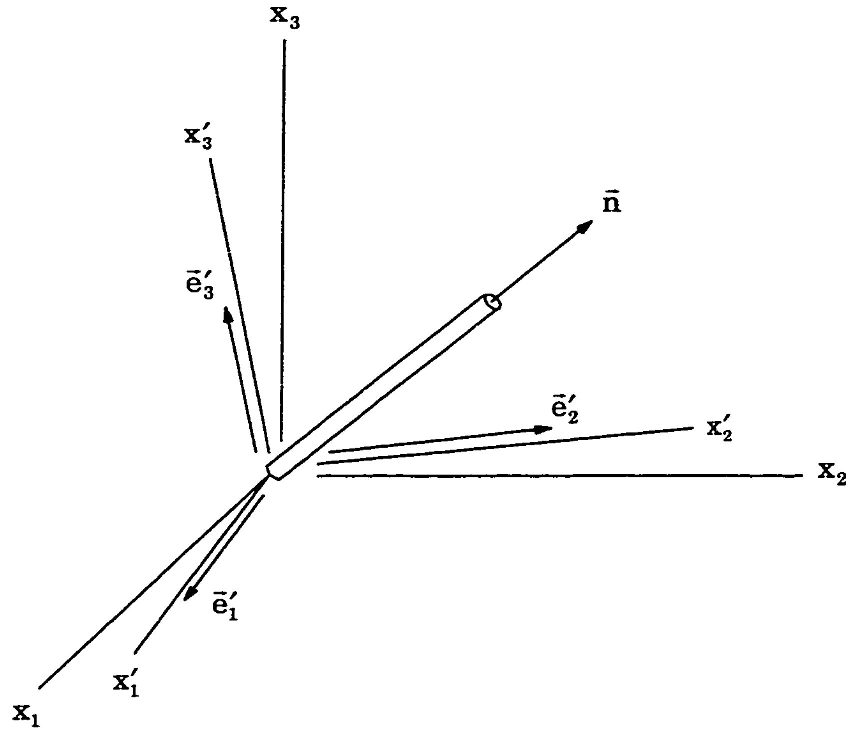

Figure 3.1 - Filamentary Silicon Conductor

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and future indicial notation expressions, the summation convention is implied for repeated indices, and reduced index notation has been used for the stress components:

$$\begin{aligned} \sigma'_1 &= \sigma'_{11}, \quad \sigma'_2 = \sigma'_{22}, \quad \sigma'_3 = \sigma'_{33} \\ \sigma'_4 &= \sigma'_{13}, \quad \sigma'_5 = \sigma'_{23}, \quad \sigma'_6 = \sigma'_{12} \end{aligned} \tag{3.2}$$

The 36 off-axis piezoresistive coefficients in Eq. (3.1) are related to the three unique on-axis piezoresistive coefficients $\pi_{11}, \pi_{12}, \pi_{44}$ (evaluated in the unprimed coordinate system aligned with the crystallographic axes) using the transformation

$$\pi'_{\alpha\beta} = T_{\alpha\gamma}\,\pi_{\gamma\delta}\,T^{-1}_{\delta\beta} \tag{3.3}$$

where

$$[\pi_{ij}] = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \tag{3.4}$$

is the on-axis piezoresistive coefficient matrix, and

$$[T_{\alpha\beta}] = \begin{bmatrix} l_1^2 & m_1^2 & n_1^2 & 2\,l_1 n_1 & 2\,m_1 n_1 & 2\,l_1 m_1 \\ l_2^2 & m_2^2 & n_2^2 & 2\,l_2 n_2 & 2\,m_2 n_2 & 2\,l_2 m_2 \\ l_3^2 & m_3^2 & n_3^2 & 2\,l_3 n_3 & 2\,m_3 n_3 & 2\,l_3 m_3 \\ l_1 l_3 & m_1 m_3 & n_1 n_3 & l_1 n_3 + l_3 n_1 & m_1 n_3 + m_3 n_1 & l_1 m_3 + l_3 m_1 \\ l_2 l_3 & m_2 m_3 & n_2 n_3 & l_2 n_3 + l_3 n_2 & m_2 n_3 + m_3 n_2 & l_2 m_3 + l_3 m_2 \\ l_1 l_2 & m_1 m_2 & n_1 n_2 & l_1 n_2 + l_2 n_1 & m_1 n_2 + m_2 n_1 & l_1 m_2 + l_2 m_1 \end{bmatrix} \tag{3.5}$$

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is the six by six transformation matrix whose elements are related to the direction cosines of the primed coordinate directions with respect to the unprimed coordinate directions. The inverse of this transformation matrix can be expressed as:

$$[T_{\alpha\beta}]^{-1} = \begin{bmatrix} l_1^2 & l_2^2 & l_3^2 & 2 l_1 l_3 & 2 l_2 l_3 & 2 l_1 l_2 \\ m_1^2 & m_2^2 & m_3^2 & 2 m_1 m_3 & 2 m_2 m_3 & 2 m_1 m_2 \\ n_1^2 & n_2^2 & n_3^2 & 2 n_1 n_3 & 2 n_2 n_3 & 2 n_1 n_2 \\ l_1 n_1 & l_2 n_2 & l_3 n_3 & l_1 n_3 + l_3 n_1 & l_2 n_3 + l_3 n_2 & l_1 n_2 + l_2 n_1 \\ m_1 n_1 & m_2 n_2 & m_3 n_3 & m_1 n_3 + m_3 n_1 & m_2 n_3 + m_3 n_2 & m_1 n_2 + m_2 n_1 \\ l_1 m_1 & l_2 m_2 & l_3 m_3 & l_1 m_3 + l_3 m_1 & l_2 m_3 + l_3 m_2 & l_1 m_2 + l_2 m_1 \end{bmatrix} \quad (3.6)$$

In Eqs. (3.5, 3.6), the direction cosines for the axes of the primed coordinate system are given by

$$[a_{ij}] = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} \quad (3.7)$$

where

$$a_{ij} = \cos(x'_i, x_j) \quad (3.8)$$

When the primed axes are aligned with the unprimed (crystallographic) axes, the transformation matrix in Eq. (3.5) reduces to the 6 x 6 identity matrix. Thus, Eq. (3.3) reduces to

$$\pi'_{\alpha\beta} = \pi_{\alpha\beta} \quad (3.9)$$

and Eq. (3.1) simplifies to

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$$\frac{\Delta R}{R} = [\pi_{11}\sigma_{11} + \pi_{12}(\sigma_{22} + \sigma_{33})]l^2 + [\pi_{11}\sigma_{22} + \pi_{12}(\sigma_{11} + \sigma_{33})]m^2 + [\pi_{11}\sigma_{33} + \pi_{12}(\sigma_{11} + \sigma_{22})]n^2 + 2\pi_{44}[\sigma_{12}lm + \sigma_{13}ln + \sigma_{23}mn] + [\alpha_1 T + \alpha_2 T^2 + ...] \tag{3.10}$$

where l, m, n are the direction cosines of the conductor orientation with respect to the unprimed (crystallographic) axes. Eq. (3.10) demonstrates that the resistance change of an arbitrarily oriented silicon resistor depends on all six stress components. As will be shown below, resistive sensor rosettes can be fabricated in certain silicon wafer planes which take advantage of this property and allow several stress components to be extracted from monitoring resistance changes.

3.2 Resistance Change Equations for Silicon Wafer Planes

For a given wafer orientation, Eq. (3.1) can be used to obtain the resistance change equation for an arbitrarily oriented in-plane resistor. In the current microelectronics industry, it is most common for silicon devices to be fabricated using (100) silicon wafers. A general (100) silicon wafer is shown in Figure 3.2. The surface of the wafer is a (100) plane, and the [001] direction is normal to the wafer plane. The axes of the natural wafer coordinate system $x_1' = [110]$ and $x_2' = [\bar{1}10]$ are parallel and perpendicular to the primary wafer flat. To use Eq. (3.1), the off-axis piezoresistive coefficients in the primed coordinate system must be evaluated using Eq. (3.3) by substitution of the unprimed values in Eq. (3.4) and the appropriate direction cosines. For the unprimed and primed coordinate systems shown in Figure 3.2, the direction cosines are:

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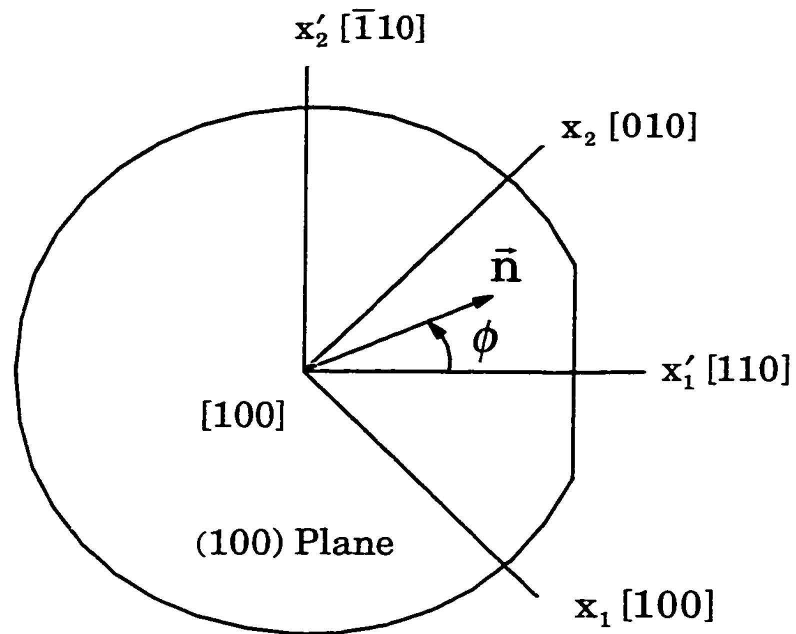

Figure 3.2 - (100) Silicon Wafer

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$$[a_{ij}] = \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{3.11}$$

Substitution of the off-axis piezoresistive coefficients calculated in the manner described above into Eq. (3.1) yields

$$\begin{aligned} \frac{\Delta R}{R} = & \left[\left(\frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \right) \sigma'_{11} + \left(\frac{\pi_{11} + \pi_{12} - \pi_{44}}{2} \right) \sigma'_{22} \right] \cos^2\phi \\ & + \left[\left(\frac{\pi_{11} + \pi_{12} - \pi_{44}}{2} \right) \sigma'_{11} + \left(\frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \right) \sigma'_{22} \right] \sin^2\phi \\ & + \pi_{12}\sigma'_{33} + (\pi_{11} - \pi_{12})\sigma'_{12}\sin 2\phi + [\alpha_1 T + \alpha_2 T^2 \ + \ldots] \end{aligned} \tag{3.12}$$

where

$$l' = \cos\phi \qquad m' = \sin\phi \qquad n' = 0 \tag{3.13}$$

has been introduced, and ϕ is the angle between the x'_1-axis and the resistor orientation. Equation (3.12) indicates that the out-of-plane shear stresses σ'_{13} and σ'_{23} do not influence the resistances of stress sensors fabricated on (100) wafers. This means that a sensor rosette on (100) silicon can at best measure four of the six unique components of the stress tensor. All three of the unique piezoresistive coefficients for silicon $(\pi_{11}, \pi_{12}, \pi_{44})$ appear in Eq. (3.12). These parameters must be calibrated before stress component values can be extracted from resistance change measurements.

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The other common silicon crystal orientation used in semiconductor fabrication is the (111) surface. A general (111) silicon wafer is shown in Figure 3.3. The surface of the wafer is a (111) plane, and the [111] direction is normal to the wafer plane. The principal crystallographic axes x_1 = [100], x_2 = [010], and x_3 = [001] do not lie in the wafer plane and have not been indicated. As mentioned previously, it is convenient to work in an off-axis primed wafer coordinate system where the axes x'_1, x'_2 are parallel and perpendicular to the primary wafer flat. Using Eq. (3.1), the resistance change of an arbitrarily oriented in-plane sensor can be expressed in terms of the stress components resolved in this natural wafer coordinate system. The off-axis piezoresistive coefficients in the primed coordinate system must be first evaluated by substituting the unprimed values given in Eq. (3.4) and the appropriate direction cosines for the primed coordinate directions with respect to the unprimed (crystallographic) coordinate directions into the transformation relations given in Eq. (3.3). For the primed coordinate system indicated in Figure 3.3, the appropriate direction cosines for the primed axes are

$$[a_{ij}] = \begin{bmatrix} -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & \frac{2}{\sqrt{6}} \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \qquad (3.14)$$

Substitution of the off-axis piezoresistive coefficients, calculated in the manner described above, into Eq. (3.1) yields

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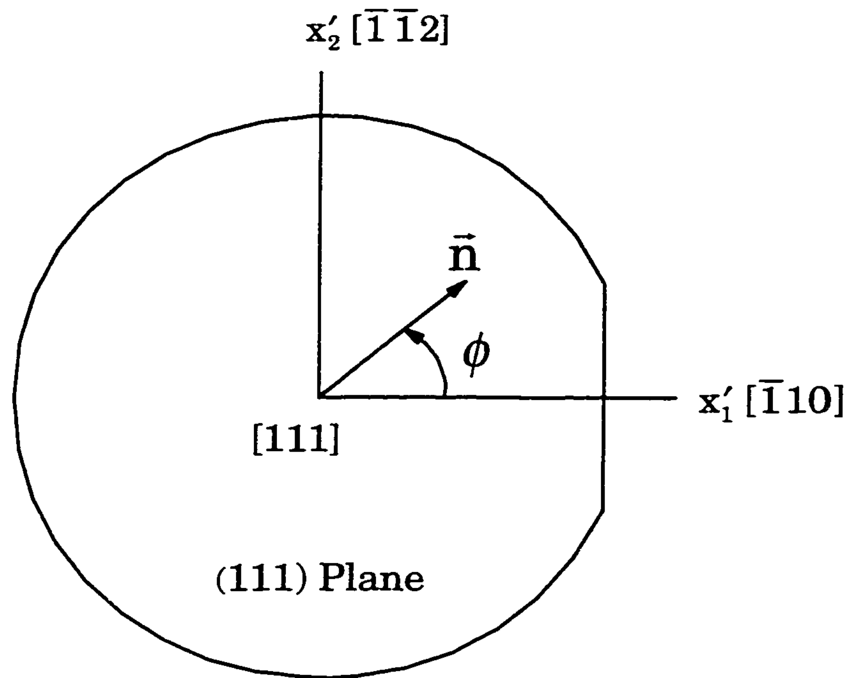

Figure 3.3 - (111) Silicon Wafer

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$$\frac{\Delta R}{R} = [B_1\sigma'_{11} + B_2\sigma'_{22} + B_3\sigma'_{33} + 2\sqrt{2}(B_2 - B_3)\sigma'_{23}]\cos^2\phi$$
$$+ [B_2\sigma'_{11} + B_1\sigma'_{22} + B_3\sigma'_{33} - 2\sqrt{2}(B_2 - B_3)\sigma'_{23}]\sin^2\phi$$
$$+ [2\sqrt{2}(B_2 - B_3)\sigma'_{13} + (B_1 - B_2)\sigma'_{12}]\sin 2\phi$$
$$+ [\alpha_1 T + \alpha_2 T^2 + \ldots] \tag{3.15}$$

where ϕ is again the angle between the x'_1-axis and the resistor orientation. The coefficients

$$B_1 = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2}$$
$$B_2 = \frac{\pi_{11} + 5\pi_{12} - \pi_{44}}{6} \tag{3.16}$$
$$B_3 = \frac{\pi_{11} + 2\pi_{12} - \pi_{44}}{3}$$

are a set of linearly independent temperature dependent combined piezoresistive parameters. These parameters must be calibrated before stress component values can be extracted from resistance change measurements. Eq. (3.15) indicates that the resistance change for a resistor in the (111) plane is dependent on all six of the unique stress components. Therefore, the potential exists for developing a sensor rosette which can measure the complete three-dimensional state of stress at points on the surface of a die.

Besides the ability to measure two additional stress components, theoretical analysis has established that properly designed sensor rosettes on the (111) silicon wafer plane have other advantages relative to sensors fabricated using standard (100) silicon [81, 82, 115]. In particular, optimized sensors on (111) silicon are capable of measuring four temperature compensated combined stress components, while those on (100) silicon can only be used to measure two temperature compensated quantities. In this discussion,

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temperature compensated refers to the ability to extract the stress components directly from the resistance change measurements (without the need to know the temperature change T). This is a particularly important attribute, given the large errors which can be introduced into non-temperature compensated stress sensor data when the temperature change T is not precisely known. Furthermore, it has been established that the (111) plane offers the opportunity to measure the highest number (four) of stress components in a temperature compensated manner (considering all possible silicon wafer orientations). The four stress components which can be measured in a temperature compensated manner using (111) silicon sensors are the three shear stress components and the difference of the in-plane normal stress components.

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CHAPTER 4

OPTIMIZED PIEZORESISTIVE SILICON TEST CHIPS

4.1 (100) Silicon Test Chip (AAA2)

In some of the packaging stress studies in this work, special (100) silicon test chips (AU/AAA2) incorporating an array of optimized calibration and measurement rosettes, and containing perimeter pads suitable for wire bonding were utilized. A schematic of the basic die image (150 x 150 mils) is shown in Figure 4.1. It contains an array of optimized four-element dual-polarity sensor rosettes for stress measurement. As shown in Figure 4.2, these rosettes contain a 0-90 p-type resistor pair and a ± 45 n-type resistor pair. It has been demonstrated [115, 125-127, 133], that this choice of sensor orientations minimizes thermally induced errors as well as those due to resistor misalignment, maximizes stress sensitivity, and permits accurate temperature compensated measurement of the values of the in-plane normal stress difference $\sigma'_{11} - \sigma'_{22}$ and in-place shear stress σ'_{12}.

Application of Eq. (3.12) to the various resistor orientations gives the following relations between the resistance changes and the thermally induced stresses at the rosette site:

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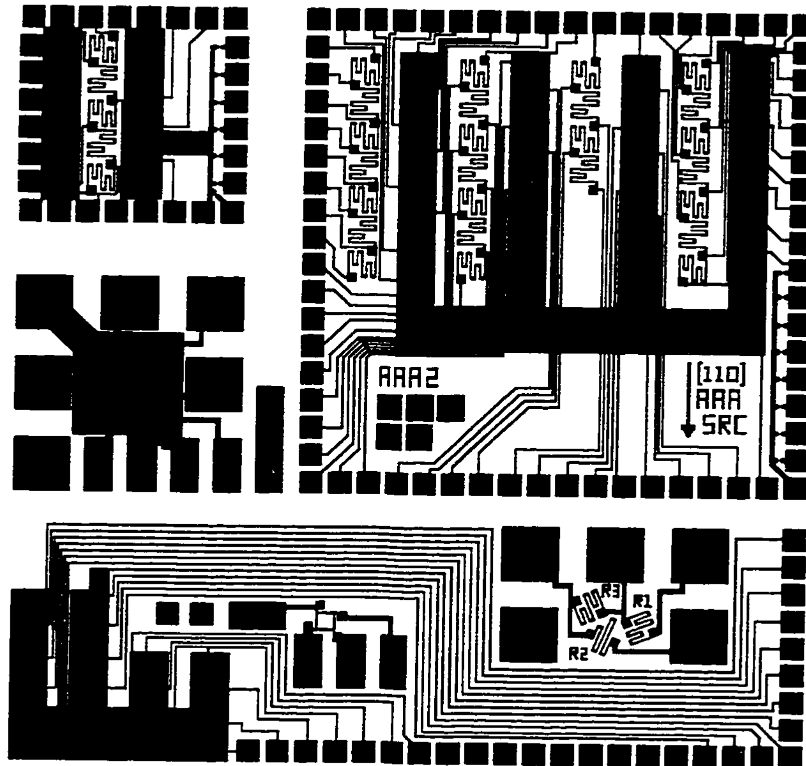

Figure 4.1 - AAA2 (100) Silicon Test Chip

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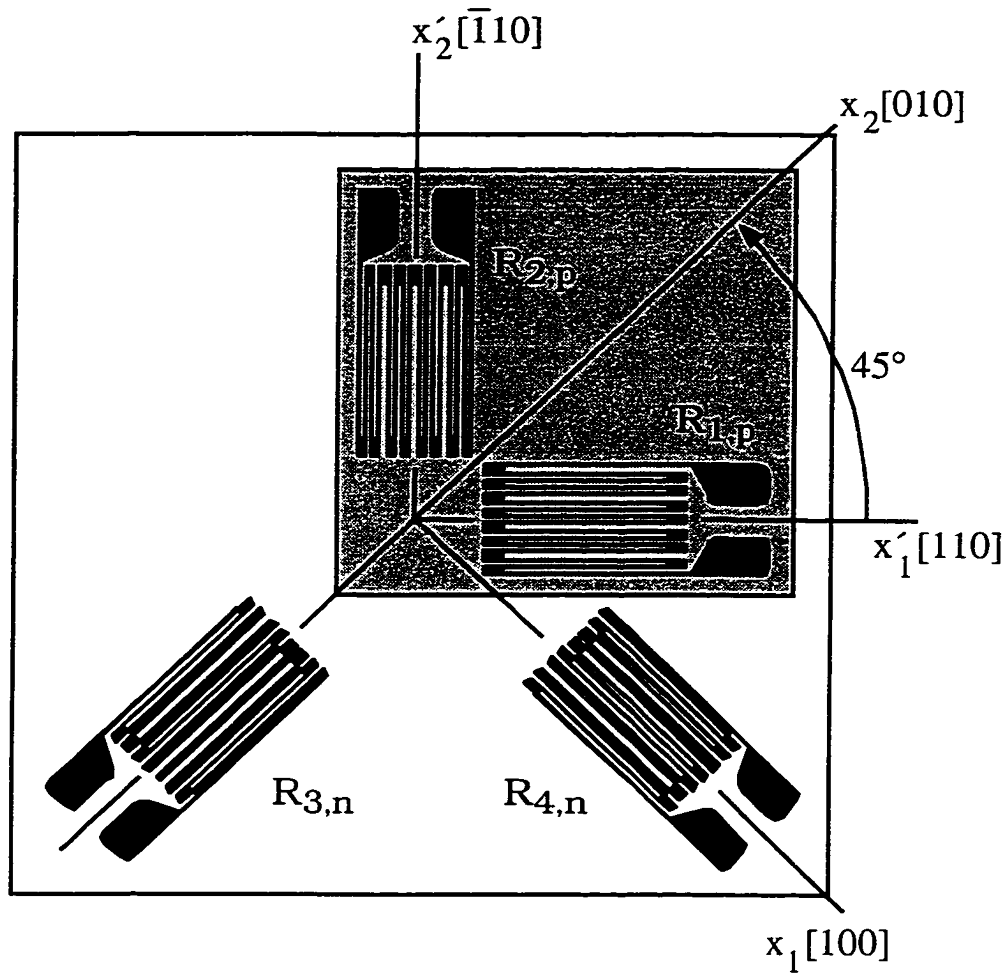

Figure 4.2 - Optimized Measurement Rosette

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$$\frac{\Delta R_1}{R_1} = \frac{\left(\pi_S^p + \pi_{44}^p\right)}{2}\sigma'_{11} + \frac{\left(\pi_S^p - \pi_{44}^p\right)}{2}\sigma'_{22} + \pi_{12}^p \sigma'_{33} + \alpha_1^p T$$

$$\frac{\Delta R_2}{R_2} = \frac{\left(\pi_S^p - \pi_{44}^p\right)}{2}\sigma'_{11} + \frac{\left(\pi_S^p + \pi_{44}^p\right)}{2}\sigma'_{22} + \pi_{12}^p \sigma'_{33} + \alpha_1^p T$$

$$\frac{\Delta R_3}{R_3} = \pi_S^n\left(\sigma'_{11} + \sigma'_{22}\right) + \pi_D^n \sigma'_{12} + \pi_{12}^n \sigma'_{33} + \alpha_1^n T \tag{4.1}$$

$$\frac{\Delta R_4}{R_4} = \pi_S^n\left(\sigma'_{11} + \sigma'_{22}\right) - \pi_D^n \sigma'_{12} + \pi_{12}^n \sigma'_{33} + \alpha_1^n T$$

where the notations $\pi_s = (\pi_{11} + \pi_{22})$ and $\pi_D = (\pi_{11} - \pi_{12})$ have been introduced. In the above equations, superscripts n and p are used on piezoresistive coefficients to denote n-type and p-type resistors, respectively. Combination of the formulas in Eq. (4.1) leads to two temperature compensated resistance stress expressions:

$$\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2} = \pi_{44}^p(\sigma'_{11} - \sigma'_{22})\frac{\Delta R_1}{R_1}$$

$$\frac{\Delta R_4}{R_4} - \frac{\Delta R_3}{R_3} = 2\pi_D^n \sigma'_{12} \tag{4.2}$$

Also included in the basic die image are two types of three-element off-axis 0-45°-90° rosettes, optimized for uniaxial calibration of required piezoresistive coefficients: π_{44} of p-type silicon and $\pi_D = \pi_{11} - \pi_{22}$ of n-type silicon [126]. The uniaxial calibration procedure requires the unusual use of special off-axis wafer stripes cut at an angle of 22.5° relative to the line normal to the wafer flat. Large area bonding pads are

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used for the calibration rosettes to facilitate probing or bonding of large diameter aluminum wires.

The basic die image in Figure 4.1 can be arrayed to obtain larger test chips. In this case, access is only available to sensors which are interconnected to pads on the perimeter of the arrayed die. The basic 150 x 150 mil die image also contains 50 x 50 mil and 100 x 100 mil sub-images for use in stress studies involving smaller die. A fully ion-implanted process has been used to fabricate the n- and p-type resistors/sensors. Process simulations were used to optimize the fabrication so that relatively large values of the sensor resistances and piezoresistive coefficients were achieved. A photograph of some of the measurement rosettes on one of the fabricated test chips is shown in Figure 4.3. The sensor rosettes on the (100) test chips have been calibrated using on-axis and off-axis four-point bending [123, 125-126,], wafer level [129], and hydrostatic [82, 131] calibration methods. Several calibration techniques were used for each piezoresistive coefficient to provide redundant checks on the measured values. For the AAA-2 test chip rosettes in this study, average values of $\pi_{44}^{p} = 1107\,(1/\text{TPa})$ and $\pi_{D}^{n} = -850\,(1/\text{TPa})$ were obtained.

4.2 (111) Silicon Test Chips (BMW-1 and BMW-2)

4.2.1 Optimized Eight-Element Rosette

The (111) silicon eight-element dual polarity rosette in Figure 4.4 has been developed at Auburn University for measurement of the complete state of stress at points on the surface of a packaged semiconductor die. It has been optimized to measure all six stress components (four in a temperature compensated manner). It can be readily

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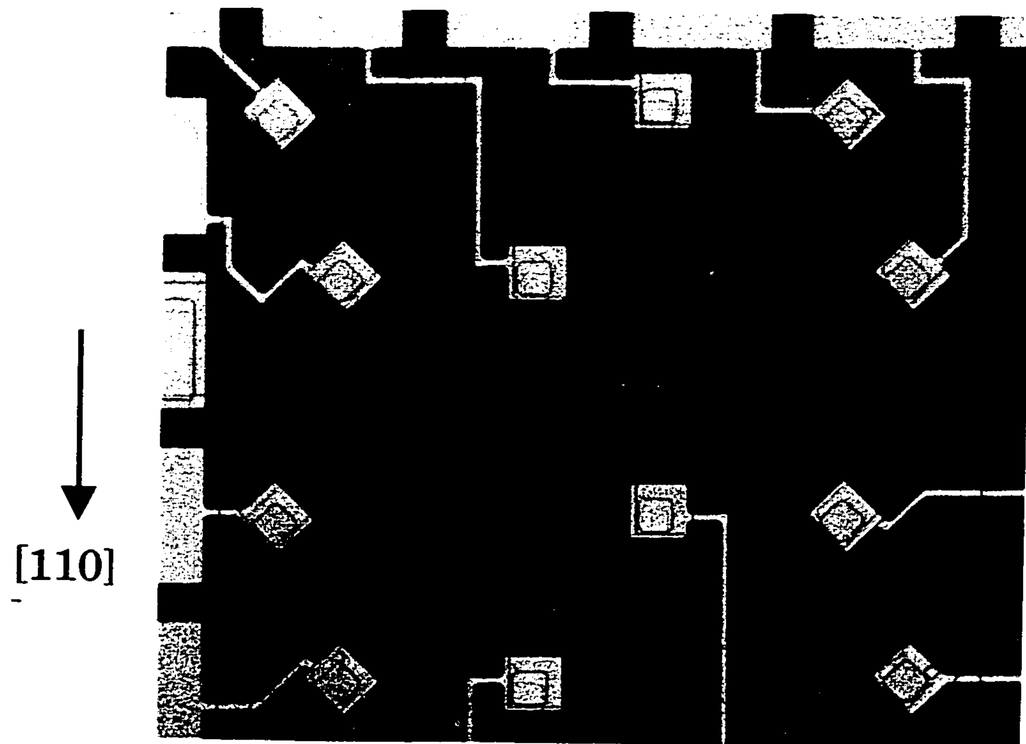

Figure 4.3 - Fabricated Measurement Rosettes on the AAA-2 Test Chip

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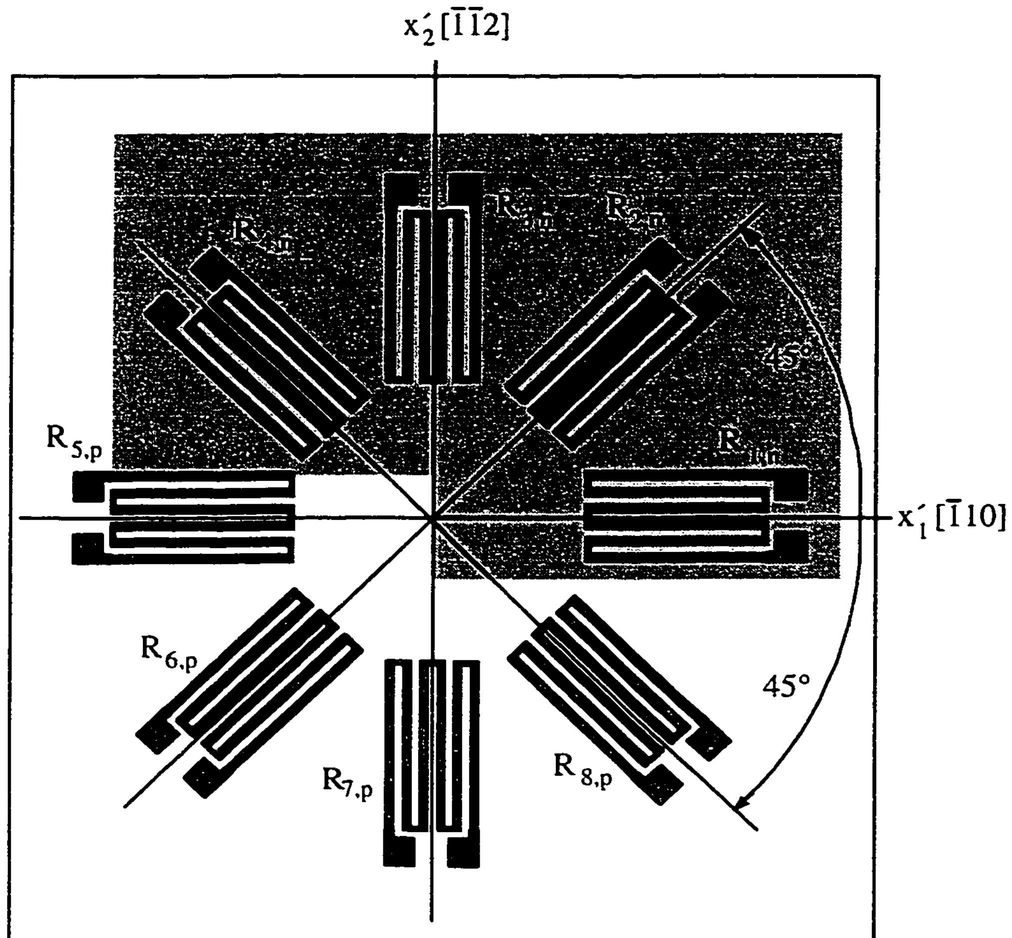

Figure 4.4 - Optimized Eight Element Rosette on (111) Silicon

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calibrated using uniaxial and hydrostatic testing. A six element rosette (without the -45° resistors) can also be used to extract the complete stress state. However, including the two extra resistors allows for more convenient bridge measurements of the resistance changes and better stress measurement localization [82].

The rosette in Figure 4.4 contains p-type and n-type sensor sets, each with resistor elements making angles of $\phi = 0, \pm 45°, 90°$ with respect to the x'_1-axis. Use of both p-type and n-type sensors is required to measure more than three stress components [35] since there are only three unique resistance changes for a set of sensors of one doping type/level which are fabricated in a single plane. Repeated application of Eq. (3.15) to each of the piezoresistive sensing elements leads to the following expressions for the stress-induced resistance changes:

$$
\begin{aligned}
\frac{\Delta R_1}{R_1} &= B_1^n \sigma'_{11} + B_2^n \sigma'_{22} + B_3^n \sigma'_{33} + 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{23} \\
&\quad + [\alpha_1^n T + \alpha_2^n T^2 + \ldots] \\
\frac{\Delta R_2}{R_2} &= \left(\frac{B_1^n + B_2^n}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^n \sigma'_{33} + 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{13} \\
&\quad + (B_1^n - B_2^n)\sigma'_{12} + [\alpha_1^n T + \alpha_2^n T^2 + \ldots] \\
\frac{\Delta R_3}{R_3} &= B_2^n \sigma'_{11} + B_1^n \sigma'_{22} + B_3^n \sigma'_{33} - 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{23} \\
&\quad + [\alpha_1^n T + \alpha_2^n T^2 + \ldots] \\
\frac{\Delta R_4}{R_4} &= \left(\frac{B_1^n + B_2^n}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^n \sigma'_{33} - 2\sqrt{2}(B_2^n - B_3^n)\sigma'_{13} \\
&\quad - (B_1^n - B_2^n)\sigma'_{12} + [\alpha_1^n T + \alpha_2^n T^2 + \ldots]
\end{aligned}
\tag{4.3}
$$

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$$\frac{\Delta R_5}{R_5} = B_1^p\sigma_{11} + B_2^p\sigma'_{22} + B_3^p\sigma'_{33} + 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{23} + [\alpha_1^pT + \alpha_2^pT^2 + \ldots]$$

$$\frac{\Delta R_6}{R_6} = \left(\frac{B_1^p + B_2^p}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^p\sigma'_{33} + 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{13} + (B_1^p - B_2^p)\sigma'_{12} + [\alpha_1^pT + \alpha_2^pT^2 + \ldots]$$

$$\frac{\Delta R_7}{R_7} = B_2^p\sigma'_{11} + B_1^p\sigma'_{22} + B_3^p\sigma'_{33} - 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{23} + [\alpha_1^pT + \alpha_2^pT^2 + \ldots] \tag{4.3}$$

$$\frac{\Delta R_8}{R_8} = \left(\frac{B_1^p + B_2^p}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^p\sigma'_{33} - 2\sqrt{2}(B_2^p - B_3^p)\sigma'_{13} - (B_1^p - B_2^p)\sigma'_{12} + [\alpha_1^pT + \alpha_2^pT^2 + \ldots]$$

Superscripts n and p are used on the combined piezoresistive coefficients to denote n-type and p-type resistors, respectively.

For an arbitrary state of stress, these expressions can be inverted to solve for the six stress components in terms of the measured resistance changes:

$$\sigma'_{11} = \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^nT\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^pT\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}$$

$$\sigma'_{22} = -\frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^nT\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^pT\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]} \tag{4.4}$$

$$\sigma'_{33} = \frac{-(B_1^p + B_2^p)\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^nT\right] + (B_1^n + B_2^n)\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^pT\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}$$

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$$\sigma'_{13}=\frac{\sqrt{2}}{8}\left[\frac{(B_2^p-B_1^p)\left[\frac{\Delta R_4}{R_4}-\frac{\Delta R_2}{R_2}\right]-(B_2^n-B_1^n)\left[\frac{\Delta R_8}{R_8}-\frac{\Delta R_6}{R_6}\right]}{(B_2^p-B_1^p)B_3^n+(B_1^p-B_3^p)B_2^n+(B_3^p-B_2^p)B_1^n}\right]$$

$$\sigma'_{23}=\frac{\sqrt{2}}{8}\left[\frac{-(B_2^p-B_1^p)\left[\frac{\Delta R_1}{R_1}-\frac{\Delta R_3}{R_3}\right]+(B_2^n-B_1^n)\left[\frac{\Delta R_5}{R_5}-\frac{\Delta R_7}{R_7}\right]}{(B_2^p-B_1^p)B_3^n+(B_1^p-B_3^p)B_2^n+(B_3^p-B_2^p)B_1^n}\right] \qquad (4.4)$$

$$\sigma'_{12}=\frac{-(B_3^p-B_2^p)\left[\frac{\Delta R_4}{R_4}-\frac{\Delta R_2}{R_2}\right]+(B_3^n-B_2^n)\left[\frac{\Delta R_8}{R_8}-\frac{\Delta R_6}{R_6}\right]}{2[(B_2^p-B_1^p)B_3^n+(B_1^p-B_3^p)B_2^n+(B_3^p-B_2^p)B_1^n]}$$

From the expressions in Eq. (4.4), it is clear that the extraction of the three shear stresses $\sigma'_{12}, \sigma'_{13}, \sigma'_{23}$ from the measured resistance changes is temperature compensated (independent of T). Evaluation of the normal stress components requires measurement of the normalized resistance changes of the sensors and the temperature change T experienced by the sensing elements. The temperature coefficients of resistance $\alpha_1, \alpha_2, ...$ must also be known for each doping type. They can be obtained using thermal cycling calibration experiments where the resistances of the sensing elements are monitored as a function of temperature. The measured resistance change versus temperature response is fit with a general polynomial to extract the temperature coefficients of resistance. Typically, only first and second order temperature coefficients are needed.

Jaeger, et al. [127,133] have previously discussed the difficulties in obtaining accurate temperature change values over the long time spans typical of measurements made with piezoresistive sensors (e.g. before and after die encapsulation). In addition, it has been demonstrated that temperature measurement errors of as little as .25 °C can cause serious errors in the experimental values of the stresses extracted with non temperature

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compensated formulas such as the first three expressions in eq. (4.4). Thus, it has been recommended to restrict measurement efforts to temperature compensated stress combinations where the temperature coefficient of resistance terms cancel in the stress extraction equations. Besides the three shear stresses, an additional temperature compensated quantity can be obtained by subtracting the expressions for the in-plane normal stresses σ'_{11} and σ'_{22} in Eq. (4.4):

$$\sigma'_{11} - \sigma'_{22} = \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]} \tag{4.5}$$

This result assumes that the temperature coefficients of resistance are well matched for sensing elements of the same doping type.

The expressions in Eq. (4.4) indicate that a calibration procedure must be performed to determine all six of the combined piezoresistive parameters B_1^n, B_2^n, B_3^n, B_1^p, B_2^p, B_3^p prior to using the sensor. A combination of uniaxial and hydrostatic pressure testing can be utilized to complete this task. For example, if a known uniaxial stress $\sigma'_{11} = \sigma$ is applied in the x'_1-direction, the expressions in Eq. (4.3) for the 0-90° oriented sensors yield the following resistance changes:

$$\frac{\Delta R_1}{R_1} = B_1^n \sigma + \alpha_1^n T \qquad \frac{\Delta R_3}{R_3} = B_2^n \sigma + \alpha_1^n T$$
$$\frac{\Delta R_5}{R_5} = B_1^p \sigma + \alpha_1^p T \qquad \frac{\Delta R_7}{R_7} = B_2^p \sigma + \alpha_1^p T \tag{4.6}$$

From these expressions, it is clear that the constants B_1^n, B_2^n, B_1^p, B_2^p can be easily determined through a controlled isothermal application of uniaxial stress to a sensor rosette

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while monitoring the resulting resistance changes. If a sensor rosette is subjected to hydrostatic pressure $(\sigma'_{11} = \sigma'_{22} = \sigma'_{33} = -p)$, the relations in Eq. (4.3) give:

$$\frac{\Delta R_1}{R_1} = \frac{\Delta R_2}{R_2} = \frac{\Delta R_3}{R_3} = \frac{\Delta R_4}{R_4} = -[B_1^n + B_2^n + B_3^n]p + \alpha_1^n T$$
$$\frac{\Delta R_5}{R_5} = \frac{\Delta R_6}{R_6} = \frac{\Delta R_7}{R_7} = \frac{\Delta R_8}{R_8} = -[B_1^p + B_2^p + B_3^p]p + \alpha_1^p T \tag{4.7}$$

Therefore, the combinations $(B_1^n + B_2^n + B_3^n)$ and $(B_1^p + B_2^p + B_3^p)$ can be evaluated through a controlled isothermal application of a hydrostatic pressure to a sensor rosette while monitoring the resulting resistance changes. The individual values of B_3^n and B_3^p can then be obtained by combining the hydrostatic pressure calibration results with the uniaxial stress calibration results. The calibration methods (four-point bending and hydrostatic) are illustrated in Figure 4.5.

4.2.2 Auburn BMW-1 Silicon Test chip

For packaging studies, special (111) silicon test chips (BMW-1) have been fabricated which incorporate an array of the optimized eight element dual polarity measurement rosettes shown in Figure 4.4, and contain perimeter pads suitable for wire bonding. A schematic of the basic die image (200 x 200 mils) is shown in Figure 4.6. A photograph of a rosette from one of the fabricated test chips is shown in Figure 4.7. The eight rosette elements can be configured as four two-element half-bridges in order to simplify the resistor change measurements. A fully ion-implanted process has been used to balance the n- and p-type sheet resistances and resistor values, while maintaining high sensitivity to stress. Process simulations and experimental calibration results from a

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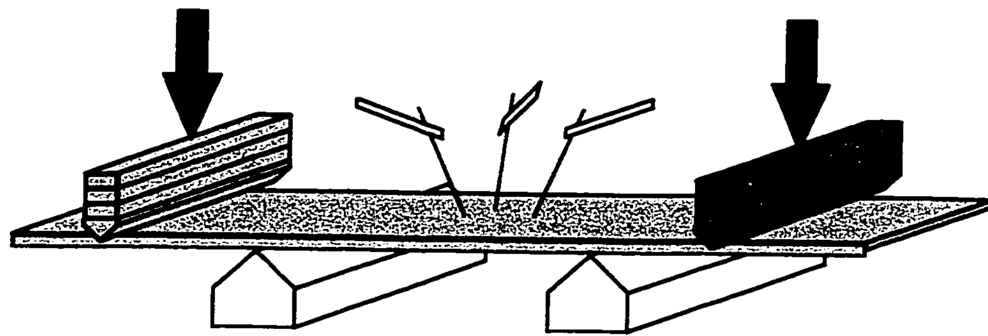
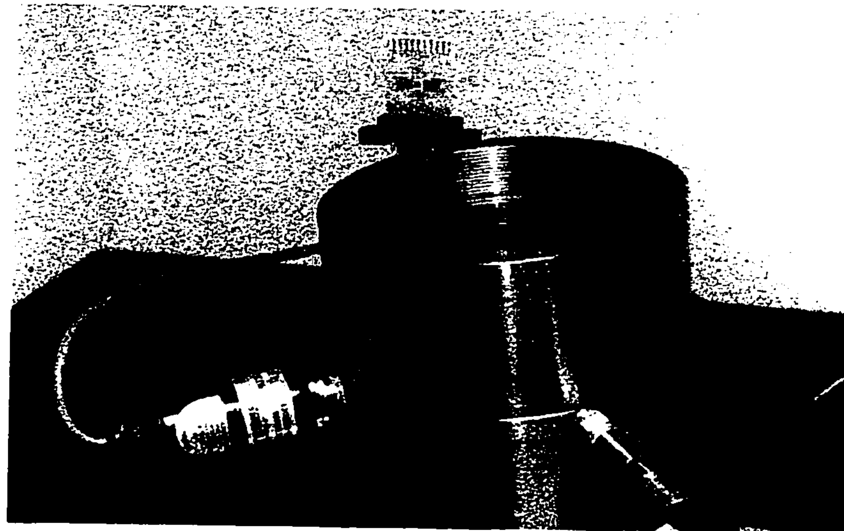


Four Point Bending



Hydrostatic

Figure 4.5 - Calibration Methods to Obtain Piezoresistive Coefficients

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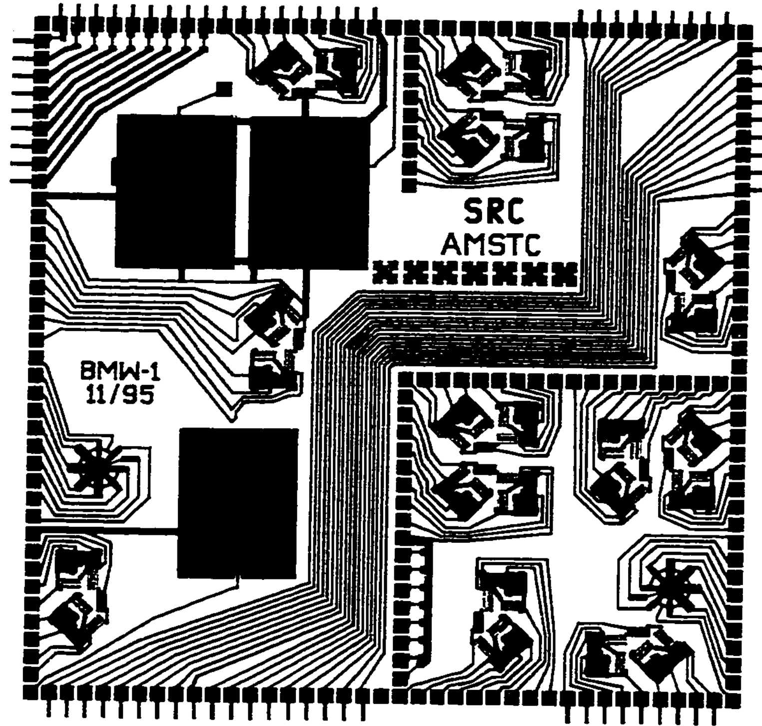

Figure 4.6 - BMW-1 Test Chip

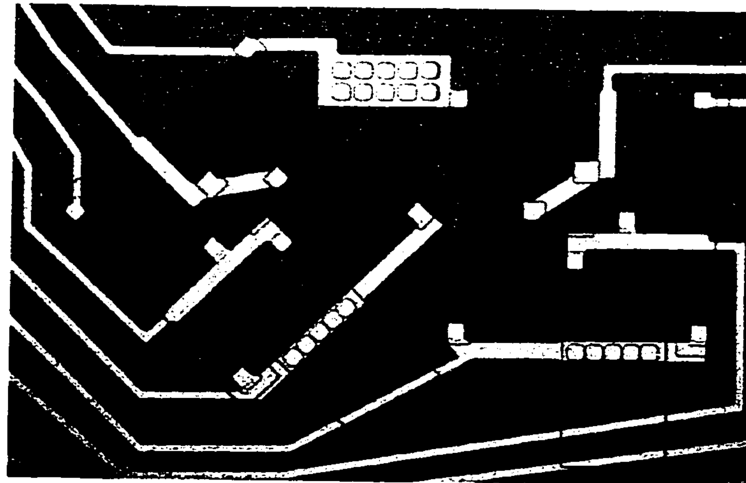

Figure 4.7 - Fabricated Rosette on BMW-1 Test Chip

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processing matrix have verified that relatively large values of the piezoresistive coefficients have been achieved.

The overall wafer image was formed by replication of the basic 200 x 200 mil die shown in Figure 4.6. The sensors on each die have been positioned to fully map the die surface stress distributions when the die is symmetrically loaded. The die are interconnected on the wafer using a special inter-chip connection pattern which permits the wafer to be cut up in multiples of 200 mils in both the horizontal and vertical directions, while maintaining access to the interior sensors across three chip boundaries. This interconnection pattern permits perimeter pad electrical access to interior sensors on die as large as 1200 x 1200 mils. The basic 200 x 200 mil die image also contains 100 x 100 mil and 100 x 200 mil subimages for use in stress studies involving smaller die.

Accurately calibrated values of six piezoresistive coefficients (B_1, B_2, and B_3 for both the p- and n-type resistors) were obtained for the utilized processing wafer conditions using controlled calibration experiments where the resistance versus stress behaviors of the rosette elements were monitored for selected mechanical loadings. In this work, the rosettes on the test chips have been calibrated using four-point bending [123], wafer level [129-130], and hydrostatic [82, 131] calibration methods. The average experimentally measured piezoresistive coefficients are tabulated in Table 4.1. Further details on the BMW-1 test chip and the calibration experiments have been presented in reference [82].

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Measured Piezoresistive Coefficients for the BMW-1 Test Chip ($\times 10^{-12}$ Pa^{-1}) (Average of 10 Rosette Sites)					
B_1^p	B_2^p	B_3^p	B_1^n	B_2^n	B_3^n
464	-130	-370	-220	193	0
Typical High End Values for Lightly Doped Silicon					
718	-228	-534	-311	298	-35

Table 4.1 - Piezoresistive Coefficient Calibration Results (BMW-1)

4.2.3 Auburn BMW-2 Silicon Test Chip

For packaging studies, special (111) silicon test chips (BMW-2) have been fabricated that incorporate an array of the optimized eight-element dual polarity measurement rosettes shown in Fig. 4.4, and that contain perimeter pads suitable for wire bonding. A schematic of the basic die image (200 x 200 mils) is shown in Fig. 4.8, and the diagram of the basic piezoresistive sensor rosette is shown in Fig. 4.9. Compared to the BMW-1 (111) silicon test chip, the BMW-2 test chip has been improved in the mapping of sensor rosettes. A calibration rosette has been introduced to facilitate four-point banding and hydrostatic calibration procedure. In addition, each rosette in the BMW-2 design requires one less bond pad than those in the BMW-1 design. Similar to the BMW-1 test chip, a fully ion-implanted p-well process has been used to balance the n- and p-type sheet resistances and resistor values, while maintaining high sensitivity to stress. A cross-sectional schematic of the resistors appears in Fig. 4.10. Process simulations and experimental calibration results from a processing matrix have been used to verify that relatively large values of the piezoresistive coefficients have been achieved. Also, the basic 200 x 200 mil die can be arrayed to form larger die. The inter-chip connections

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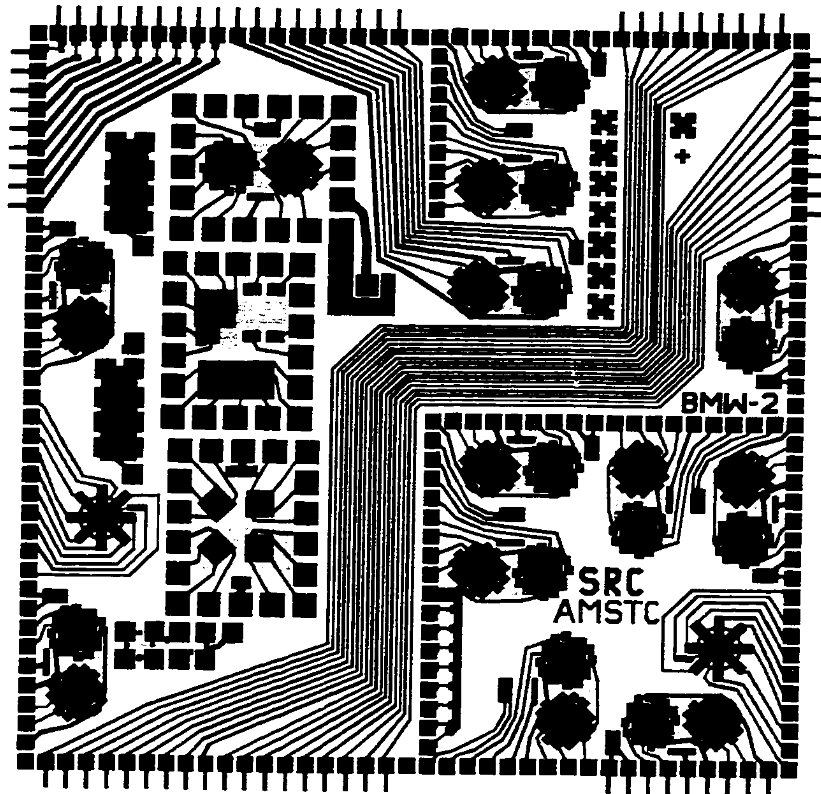

Figure 4.8 - BMW-2 Test Chip

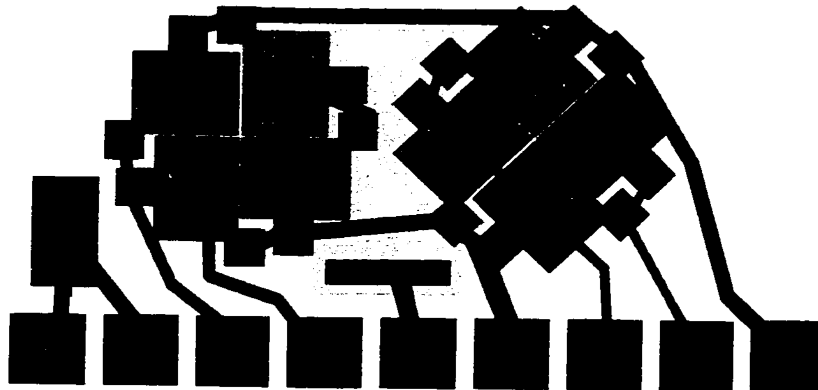

Figure 4.9 - BMW-2 Sensor Rosette

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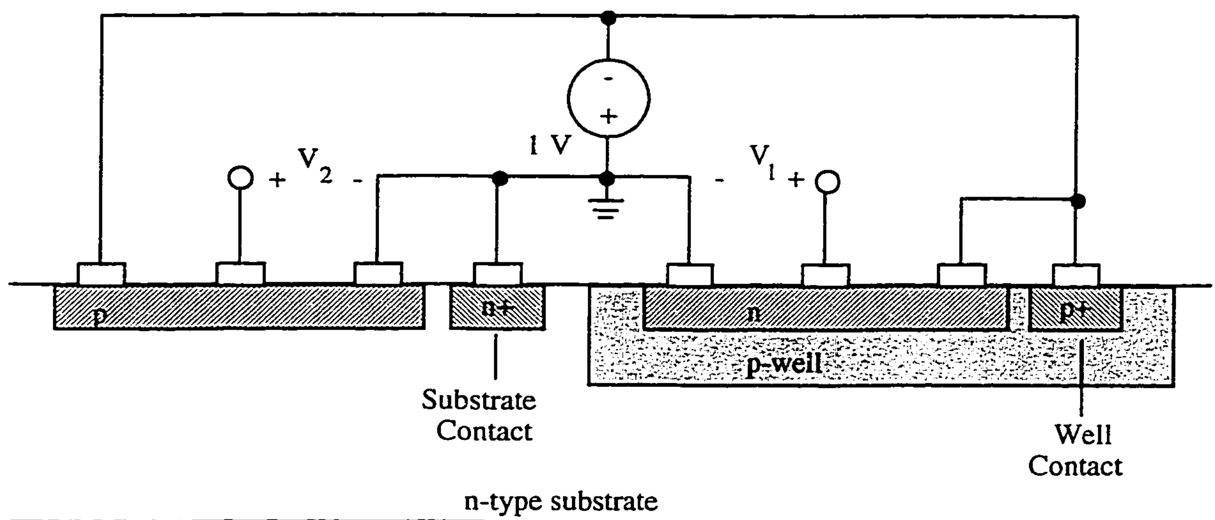

Figure 4.10 - Cross Sectional Schematic of BMW-2 Resistors

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allow for interior sensor access from the perimeter pads for die as large as 1200 mils on a side. The basic 200 x 200 mil die image also contains 100 x 100 mil and 100 x 200 mil subimages for use in stress studies involving smaller die.

Three lots of (111) silicon BMW-2 test chips have been used in the packaging stress studies discussed in later chapters. They are designated as BMW2.1, BMW2.2 and BMW2.3. Wafer lot BMW2.1 had polyimide passivation on the die surface, while wafer lots BMW2.2 and BMW2.3 both had silicon nitride passivation. Calibration procedures were performed for each batch of the wafers. As described in Chapter 4.2.1, the piezoresistive coefficients B_1 and B_2 for both the p- and n-type sensors could be obtained by using the four-point bending method, and coefficient B_3 for both the p- and n-type sensors could be extracted by means of the hydrostatic calibration technique. The calibration results for each batch of BMW-2 test chips are listed in Table 4.2-4.4.

Measured Piezoresistive Coefficients for the BMW-2 Test Chip ($\times 10^{-12}$ Pa^{-1}) (Average of 10 Rosette Sites)					
B_1^p	B_2^p	B_3^p	B_1^n	B_2^n	B_3^n
507	-145	-399	-230	207	55

Table 4.2 - Piezoresistive Coefficient Calibration Results (BMW2.1)

Measured Piezoresistive Coefficients for the BMW-2 Test Chip ($\times 10^{-12}$ Pa^{-1}) (Average of 10 Rosette Sites)					
B_1^p	B_2^p	B_3^p	B_1^n	B_2^n	B_3^n
448	-135	-351	-219	247	3.5

Table 4.3 - Piezoresistive Coefficient Calibration Results (BMW2.2)

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Measured Piezoresistive Coefficients for the BMW-2 Test Chip ($\times 10^{-12}$ Pa^{-1}) (Average of 10 Rosette Sites)					
B_1^p	B_2^p	B_3^p	B_1^n	B_2^n	B_3^n
495	-122	-411	-220	216	36.8

Table 4.4 - Piezoresistive Coefficient Calibration Results (BMW2.3)

4.2.4 TCR Mismatch Analysis

Measurements of stress over a wide range of temperature are presented in subsequent chapters using (111) silicon test chips (BMW-1 and BMW-2) based on the eight element dual polarity rosette. The accuracy of the temperature compensated extractions of the temperature dependent stress values from the sensor resistance data depends critically upon the assumption of well matched temperature coefficients of resistance made in the derivation of the expressions in Eqs. (4.4 and 4.5). If the temperature coefficients of the individual resistors in the rosette are not perfectly matched, then temperature dependent errors in the stresses will occur. These errors are

$$(\mathrm{Error})_{\sigma'_{11}-\sigma'_{22}} = \frac{(B_3^p - B_2^p)([\Delta\alpha_1^n]_{13}T + [\Delta\alpha_2^n]_{13}T^2 + \ldots) - (B_3^n - B_2^n)([\Delta\alpha_1^p]_{57}T + [\Delta\alpha_2^p]_{57}T^2 + \ldots)}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$

$$(\mathrm{Error})_{\sigma'_{12}} = \frac{-(B_3^p - B_2^p)([\Delta\alpha_1^n]_{42}T + [\Delta\alpha_2^n]_{42}T^2 + \ldots) + (B_3^n - B_2^n)([\Delta\alpha_1^p]_{86}T + [\Delta\alpha_2^p]_{86}T^2 + \ldots)}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$

$$(\mathrm{Error})_{\sigma'_{13}} = \frac{\sqrt{2}}{8}\left[\frac{(B_2^p - B_1^p)([\Delta\alpha_1^n]_{42}T + [\Delta\alpha_2^n]_{42}T^2 + \ldots) - (B_2^n - B_1^n)([\Delta\alpha_1^p]_{86}T + [\Delta\alpha_2^p]_{86}T^2 + \ldots)}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n}\right] \quad (4.8)$$

$$(\mathrm{Error})_{\sigma'_{23}} = \frac{\sqrt{2}}{8}\left[\frac{-(B_2^p - B_1^p)([\Delta\alpha_1^n]_{13}T + [\Delta\alpha_2^n]_{13}T^2 + \ldots) + (B_2^n - B_1^n)([\Delta\alpha_1^p]_{57}T + [\Delta\alpha_2^p]_{57}T^2 + \ldots)}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n}\right]$$

where $[\Delta\alpha_N]_{ij}$ is the mismatch between the Nth order temperature coefficients of resistance of resistors i and j in the eight element rosette in Figure 4.4. For a given set of TCR

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mismatches in a particular sensor rosette, the two numerator terms in each expression may either add or partially cancel.

The temperature dependence of the resistors has been carefully measured as part of the hydrostatic calibration process, and a sample of the variation of normalized resistor change with temperature for a typical set of p-type resistors appears in Figure 4.11. In this figure, the first order temperature coefficient is approximately $\alpha_1 = 500$ ppm/°C, and the coefficients of individual resistor pairs match to within 5% or better ($\Delta\alpha_1 \leq 25$ ppm/°C). Note also that the effect of the second order TCR terms is visible.

With the results from Table 4.2 and Figure 4.11, Eq. (4.8) can be used to calculate bounds on the stress measurement errors based upon worst-case choices of signs for the $\Delta\alpha$ terms. The largest potential errors were found to occur in ($\sigma'_{11} - \sigma'_{22}$). A total temperature change of 150 °C would result in errors of less than 7 MPa for ($\sigma'_{11} - \sigma'_{22}$), and in errors of less than 3.5 MPa for σ'_{12}. The maximum error estimates were found to be even less for the out-of-plane shear stresses. Thus, the errors due to mismatched temperature coefficients are assumed to be fairly small. However, the exact errors will depend upon the magnitudes and signs of the TCR mismatches in each sensor rosette.

4.3 Test Chip Application Procedure

The procedure used in this study for test chip applications includes wafer preparation, initial resistance characterization, stress sensor calibration, packaging assembly, resistance measurements after packaging, and stress calculation. In the wafer

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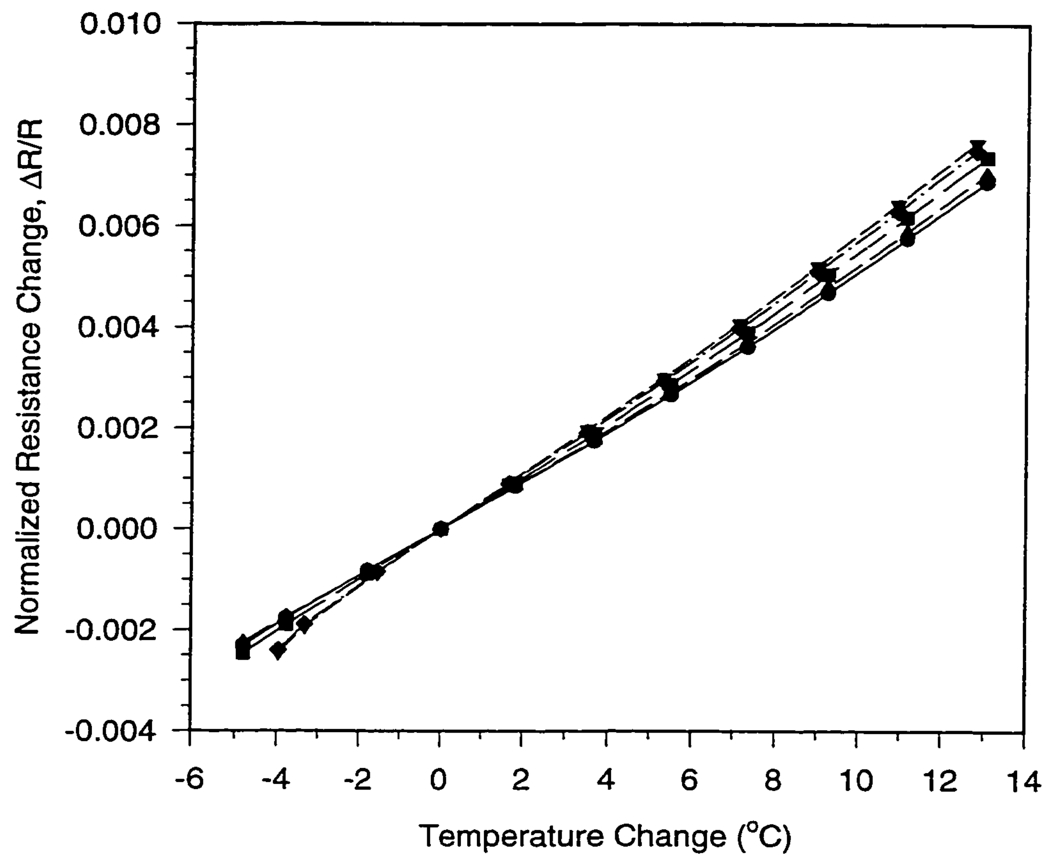

Figure 4.11 - Variation of Normalized Resistance Change with Temperature

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preparation in this work, (100) or (111) silicon test chip images were fabricated on 4 inch silicon wafers using standard CMOS microelectronic fabrication techniques. Polyimide or silicon nitride passivation was applied on the wafer surface to provide protection. Initial resistance characterization was carried out on an automated probe station. The resistance of stress sensors on the entire wafer were measured automatically through a GPIB controlled experimental setup. Some of the wafers were then sawed into strips, and four-point bending and hydrostatic calibrations were performed. The strips and remaining wafers were then diced into individual die. The characterized test chips were either sent out to a company to be packaged, or packaged in chip-on-board assemblies at Auburn. Finally, the sensor resistances in the packaged die were measured again using the same experimental setup as utilized in the initial (unstressed) resistance measurements. The stress components at the sensor rosette locations on the die surface were then extracted. Some additional details on the procedure for test chip application are reviewed below.

4.3.1 Initial Resistance Characterization

The initial resistance characterization is performed on an automated probe station. The object is to measure the resistance of each element of the sensor rosette, and identify qualified dies for application. The general characterization procedure for the BMW-2 test chip is discussed below.

The equipment involved in the characterization included:

- 1034x Probe Station

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The wafer was held on the stage of the probe station by house vacuum, and the movement of the stage was controlled by an IBM-PC compatible computer. A probe card was fixed to the probe station to provide electrical connections between the sensors on the wafer and the measurement equipment. Two types of probe cards were used in the characterization of the BMW-2 test chip. The first one was specially designed for the resistance measurements of all sensors in a single eight element rosette. The second one was used to set the binary fuse ID that identifies each individual chip.

- Computer

A computer was used to control the instrumentation for resistance measurements and ID burning through a GPIB board. The control program (1034x-4.bas) was written in Quick Basic by Robert Cordes.

- Keithley Model 617 Programmable Electrometer

The electrometer provided high resolution measurements of small currents. It was used to determine the current through the measured resistors.

- Keithley 7002 Switch System (Scanner)

The scanner was controlled to turn on or off either one or multiple channels to make the resistance measurements or chip ID burning and measurements. Two scanner cards were used for resistance measurements, and one scanner card was needed for ID burning and measurements. The detailed wiring diagram for resistance measurements will be described in Section 4.3.3.

- Power Supply

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When measuring the resistance of sensors on the BMW-2 test chip, a power supply was used to provide bias in the circuit to prevent current leakage, and to provide voltage to the measured resistors. In this study, the voltage across a resistor sensor was set to be 1V. When burning IDs for BMW2 test chip, the power supply was used to provide high current to the fuse to be blown. The voltage was usually set to be 5-10 V for ID burning.

- HP Multimeter #1

The first multimeter was used to measure the voltage applied to the sensor resistors. The reading of the multimeter should be around the bias voltage, which was set to be 1V. This voltage reading was later used for the resistance calculation. This multimeter was also used to check the chip ID. Incomplete ID burning sometimes occurs. Thus, all of the chip IDs should be checked and values recorded for future use. A 9 bit binary chip ID was used in this work. Therefore, the chip ID numbers ranged from 0 to 511. When measuring the chip ID, an open circuit (burned fuse) was labeled 1, and a short circuit (normal fuse) was labeled 0.

- HP Multimeter #2

The second multimeter was connected to a thermometer (thermistor) which was set beside the probe card and close to the wafer. In this way, the time dependent temperature change of the wafer could be recorded. Even though temperature compensated stress components were the major interest in this study, the temperature measurements served as a reference.

- House Compressed Air Line

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Compressed air was used to drive the movements of the wafer chuck in the probe station.

- House Vacuum Line

The vacuum supply was used to pick up wafers and die (vacuum pick) as well as to hold the wafer on the chuck of the probe station when taking measurement of the sensor resistances.

Figure 4.12 shows the experimental setup for test chip characterization (unstressed resistance measurements) in the wafer state on the automated probe station.

A basic BMW-2 test chip image with resistor numbering is showed in Figure 4.13. When measuring the resistances of sensors 9-24, 41-48, 73-80, the orientation of the wafer was set to be 270°, and the center of the wafer was set to be location j10 (die located at row 10 and column 10 on the wafer). When measuring the resistances of sensors 25-32 and 81-88, the orientation of the wafer was set to be 0°. After the measurements were completed, the resistance data was checked to ensure the quality of the sensors. If bad data were found in some specific die, the resistance measurements were performed again. For the BMW-2 test chip, the nominal p-type resistance value is about 11 kΩ, and the nominal n-type resistance value is around 15 kΩ. Bad sensor resistance readings might be due to poor processing during wafer fabrication or poor probe contacts. In this case, a "bad" reading is one where the value deviates greatly from the expected nominal value, or the resistance measurements are very unstable. While still in wafer state, the chip IDs were burned for subsequent identification of package samples.

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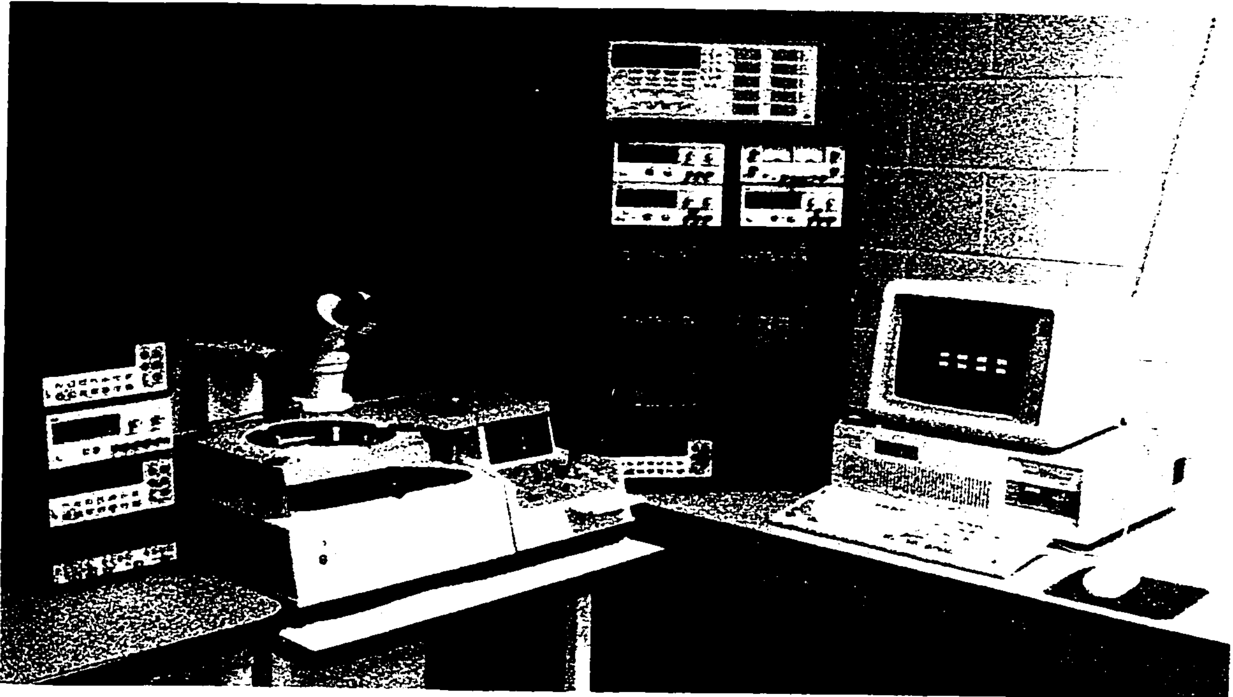

Figure 4.12 - Experimental Setup for Test Chip Characterization

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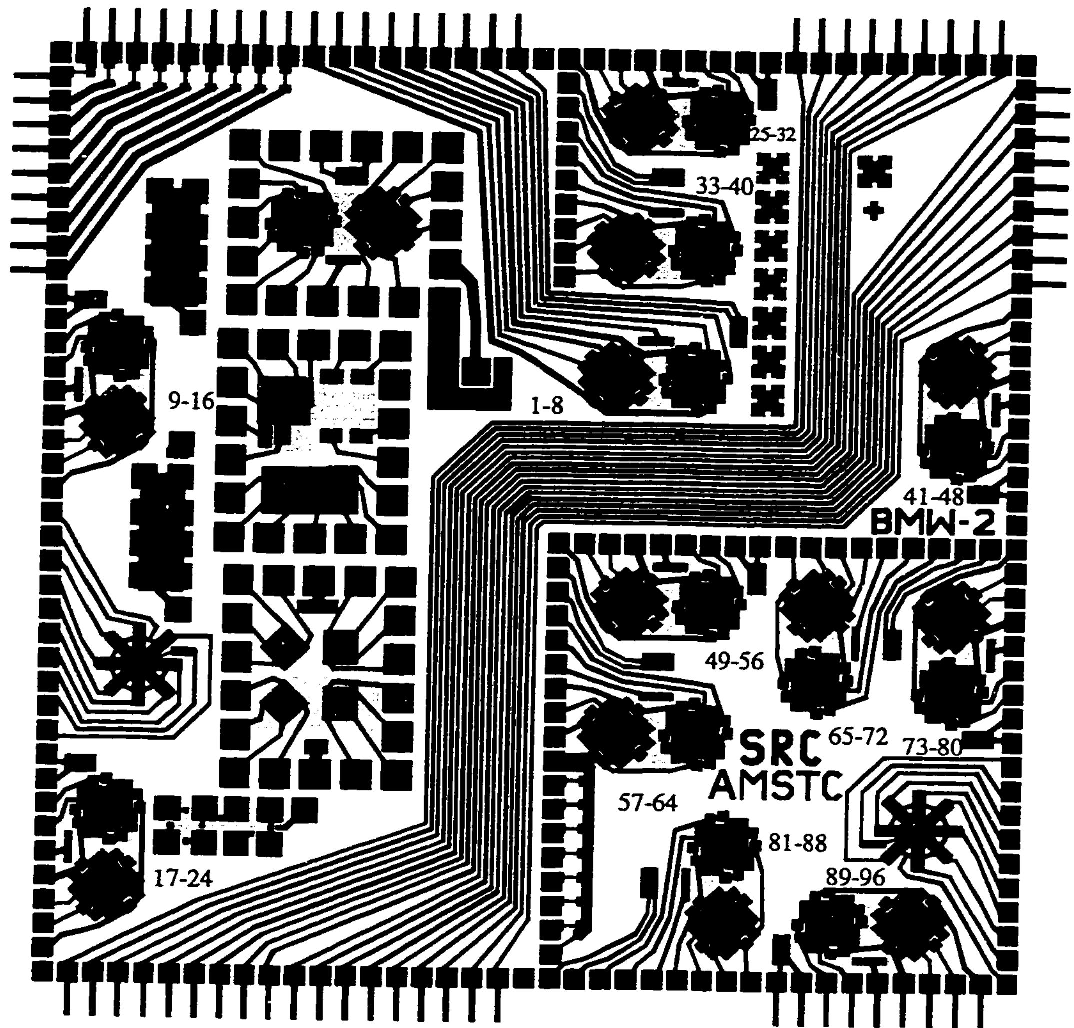

Figure 4.13 - Basic BMW-2 Test Chip with Resistor Numbering

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The internal inter-chip connections allow for larger arrayed chips in which interior sensors can be accessed from the perimeter bond pads. On the other hand, these internal connections prevent the initial resistance characterization of some sensors from being performed completely in the wafer state since the possibility exists for 2 rosettes to be simultaneously connected to the same set of band pads. Referring to Figure 4.13, this problem concerns resistors 1-8 and 89-96. One solution is to sever the inter-chip connections by cutting the wafers into strips and then later probing the effected sensors. The difficulties of making good alignment between the probes and the pads on the wafer strips cause this to be a tedious process. Another solution is to use another mask and process step to sever the unnecessary inter-chip connections. In this way, the entire wafer could be characterized thoroughly in the wafer state, and time could be saved by avoiding the tedious strip measurements. In this work, the BMW-2 chips have been used primarily in a 400 x 400 mil configuration (2 x 2 array), and a special metal layer mask was designed to sever the inter-chip connections surrounding each 400 x 400 mil die site.

After the resistance measurements were completed for all of the sensor rosettes, wafer quality maps were drawn for each wafer. These maps were used to show how many good chips were presented, and which IDs corresponded to good die. In a BMW-2 test chip wafer, a maximum of 52 chips in the 400 x 400 mil format can be obtained. The yield of the chips varied between fabrication lots, and among various wafers from the same lot.

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The wafers or strips were then diced, and qualified die were sorted and placed in waffle packs for shipment to companies to be packaged, or to be packaged locally.

Sawing of the silicon wafers into wafer strips or into individual die can cause damage. Poorly cut edges will introduce stress concentrations, and can cause die cracks and other package failures. It is essential that the blade of the diamond saw is sharp and that there is no air between the wafer and the holding tape.

4.3.2 Packaging Assembly

After the characterization and calibration procedures, the AAA-2, BMW-1, and BMW-2 test chips were assembled into various packaging configurations. In QFP, PQFP, and PLCC plastic packaging, the test chips were first attached to a lead frame. Fine gold wires were used to provide the interconnections from the die bond pads to the lead frame. The chips were then encapsulated using a mold press. Postmold encapsulant curing was conducted at a temperature higher than the glass transition temperature of the encapsulant. In ceramic PGA packaging, the test chips were bonded to the PGA packages using various die attachment adhesives. Fine aluminum wires were used to provide the interconnections from the die bond pads to the metal traces on the ceramic substrate. A lid was then used to seal the chip cavity permitting no moisture to penetrate into the package (hermetic). The various packages utilized will be described in more details in the following chapters.

Assembly of the chip-on-board packages was performed at Auburn University. Printed circuit boards were first designed and developed. The fabrication of the printed

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circuit boards included processing steps such as application of photoresist, exposure, development, etching, gold plating, etc. Detailed procedures used for making boards for the BMW-1 and BMW-2 chip-on-board samples are described in reference [134]. The die attachment adhesive was applied to the copper pad on the printed circuit board using screen printing techniques. The thickness of the die attachment material was controlled by the stencil, and was approximately 5 mils. A uniform distribution of die attachment adhesive was used to ensure stability of the samples. The test chips were then placed onto the printed circuit boards, and the die attachment adhesive was cured. Fine gold wires were used to provide the interconnections from die bond pads to metal traces on the printed circuit board. The liquid encapsulants were then dispensed on the chip and cured. The oven used for encapsulant curing had flat holding planes that allowed no movement of the encapsulant before curing.

4.3.3 Resistance Measurements after Packaging

The resistances of the sensor rosettes were measured again after the packaging processes. Using the measured resistance changes and Eqs. (4.2, 4.4, 4.5), the die stresses can be calculated. The general procedure for making after packaging resistance measurements with the BMW-2 test chips is now discussed.

The equipment utilized in the experimental procedure included:

- Computer

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A PC-based computer was used to control the instrumentation for resistance and chip ID measurements through a GPIB board. The controlled programs were written in Visual Basic, and a typical program listing is given in Appendix A.

- Keithley 7002 Switch System (Scanner)

The scanner was controlled to turn on or off either one or multiple channels to make the resistance or chip ID measurements. Up to six scanner boards were used for packaged sample measurements with a 400 x 400 mil BMW-2 test chip.

- Keithley Model 6512 Programmable Electrometer

The electrometer provided high resolution measurements of low currents. It was used to determine the current through the measured resistors.

- Power Supply

When measuring the sensor resistances on the BMW-2 test chip, a power supply was used to provide bias in the circuit to prevent current leakage, and to provide voltage to the measured resistors. In this work, the voltage across the resistor was set to be 1V.

- HP Multimeter #1

A HP multimeter was used to measure the exact voltage applied to the sensor resistors. The reading of the multimeter should be around the bias voltage, which was set to be 1V. This voltage reading was later used for the resistance calculations. This multimeter was also used to measure the chip ID. The chip ID values ranged from 0 to 511 as described in section 4.3.1. When measuring the chip ID, an open circuit was labeled as 1, and a short circuit was labeled as 0.

- HP Multimeter #2

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A second multimeter was connected to a thermometer (thermistor) that was set beside the package sample being measured. In this way, the time dependent temperature change of the assembly could be recorded. The temperature measurements were important when the packaged die surface stresses were studied as a function of temperature, or when the die surface stresses were investigated during an encapsulant cure cycle.

- Delta Design 9010 Temperature Controller

A Delta Design oven was also controlled by the computer through the GPIB board, and used to provide known temperature changes for characterization of packaging samples. The temperature was typically swept over a large range from a low temperature (as low as -60 °C) to a high temperature (as high as 170 °C). The increment of the temperature between sensor readings was usually set to be 5 °C, and the temperature at each step was maintained for at least 5 minutes before measurements were taken to ensure a uniform temperature distribution within the packaging sample.

- Accessories

Various package sockets were commercially obtained, and printed circuit boards to interface between the sockets and the scanning system were designed and fabricated. Ribbon cables and connectors (40-60 pin) were also needed to provide electrical connections between the packaged sample and the measurement equipment.

In every eight element rosette on the BMW-2 test chip there are four p-type and four n-type resistors orientated at angles of 0°, 90°, +45°, -45° from the x_1' direction. These resistors are denoted as P1, P2, P3, P4, and N1, N2, N3, N4. As shown in Figure

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4.14, the basic rosette image occurs in both horizontal and vertical formats on a test chip. When comparing the two configurations, the orientation of a particular rosette element will switch from 0° to 90° or $+45^{o}$ to -45°. In a fundamental BMW-2 (200 x 200 mil) test chip (Figure 4.15), 96 resistors are organized into 12 rosettes. Rosettes 2, 3, 6, 9, 10, 11 belong to type 1 (horizontal), and rosette 1, 4, 5, 7, 8, 12 are type 2 (vertical). Only rosettes 1, 2, 3, 4, 6, 10, 11, 12 can be reached by perimeter pads.

In Figure 4.16, the methods utilized for measuring the resistances of sensor P1 in a horizontal rosette and resistor P2 in a vertical rosette are given. The power supply provides a 1 V voltage. Referring to Figure 4.16, the electrometer serves to prevent current from entering the lower sensor, and measures the current passing through the upper sensor. Thus, the resistance of the upper sensor is simply the applied voltage of 1 V divided by the measured current.

One bank in a scanner card can be used to measure the resistances of of all sensors in one rosette. There are four banks in a scanner card. Therefore, five scanner cards are needed to measure all 20 sensor rosettes which are accessed by perimeter pads in a 400 x 400 mil BMW-2 test chip. Table 4.5 shows the connections between the bonding pads of a rosette in Figure 4.14 and the channel numbers of a bank in a scanner card.

The eight sensors in a are configured as a parallel connection of four two-element half-bridges in order to simplify the measurements of temperature compensated normalized resistance change differences. For measurements using the half-bridges, the substrate is grounded, and a bias of -1 V is applied to both the p-well and the common

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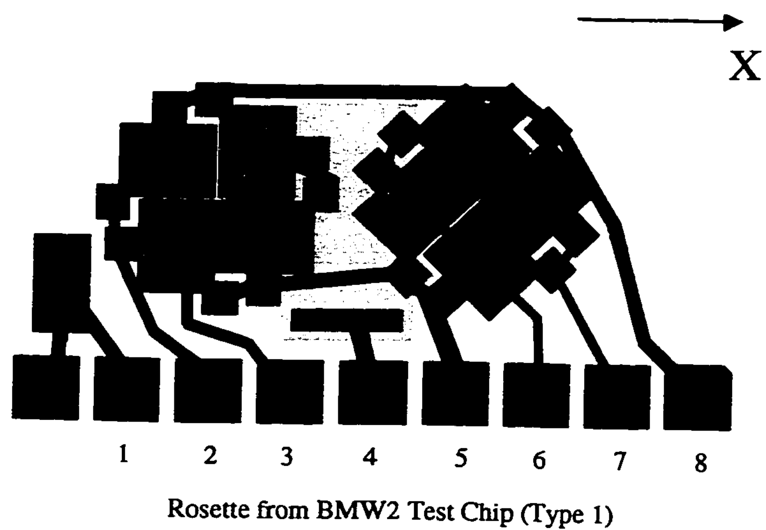
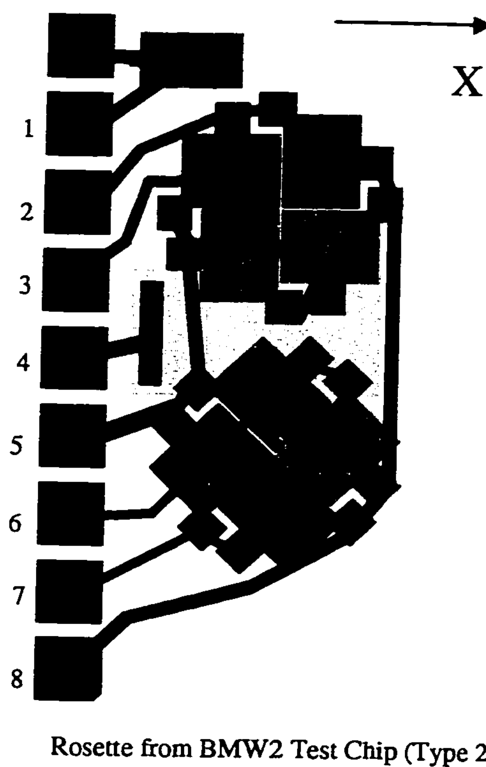


Rosette from BMW2 Test Chip (Type 1)



Rosette from BMW2 Test Chip (Type 2)

Figure 4.14 - Two Types of Rosette from BMW-2 Test Chip

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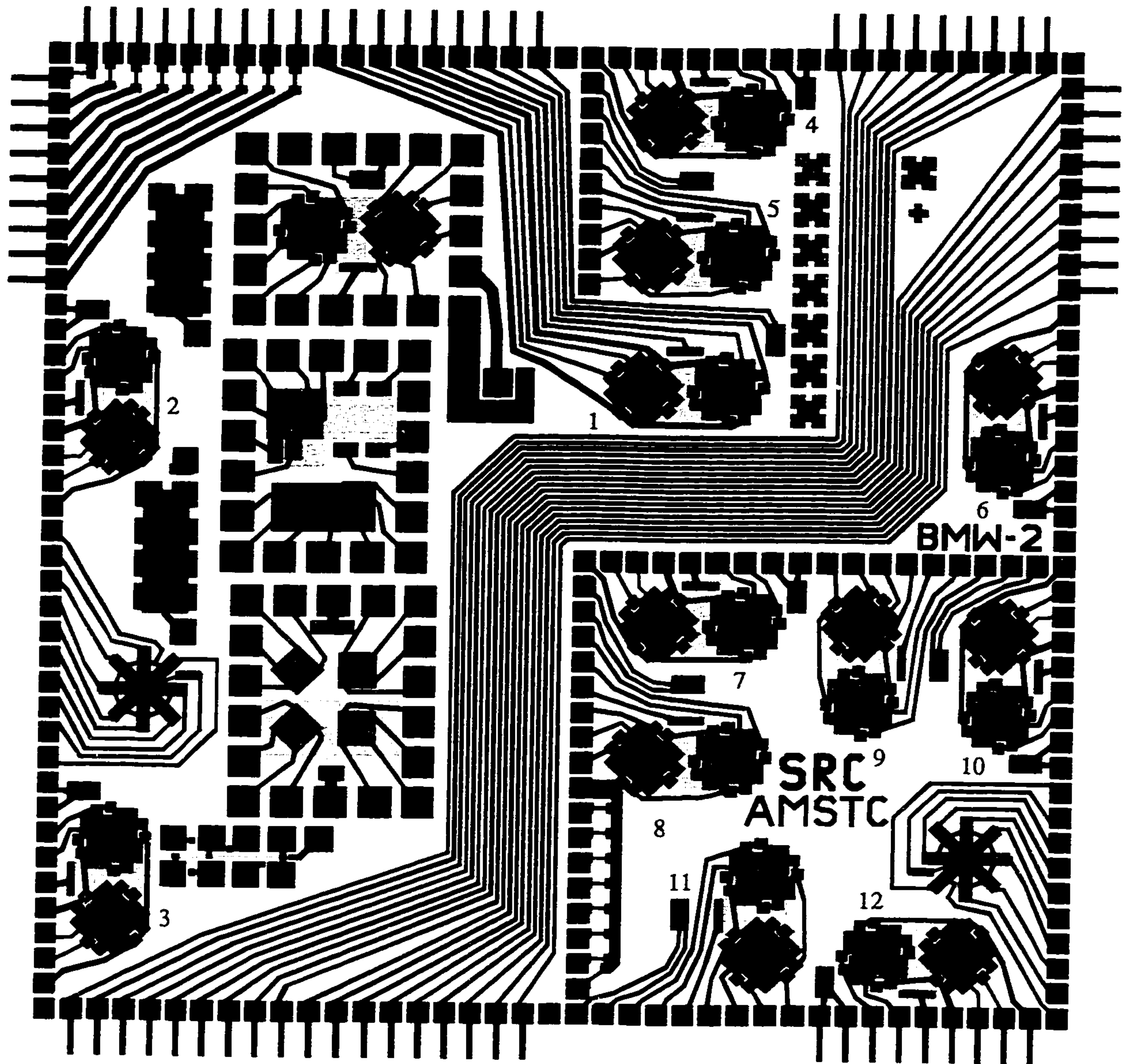

Figure 4.15 - Measurement Rosette Numbering 200 x 200 mil BMW-2 Test Chip

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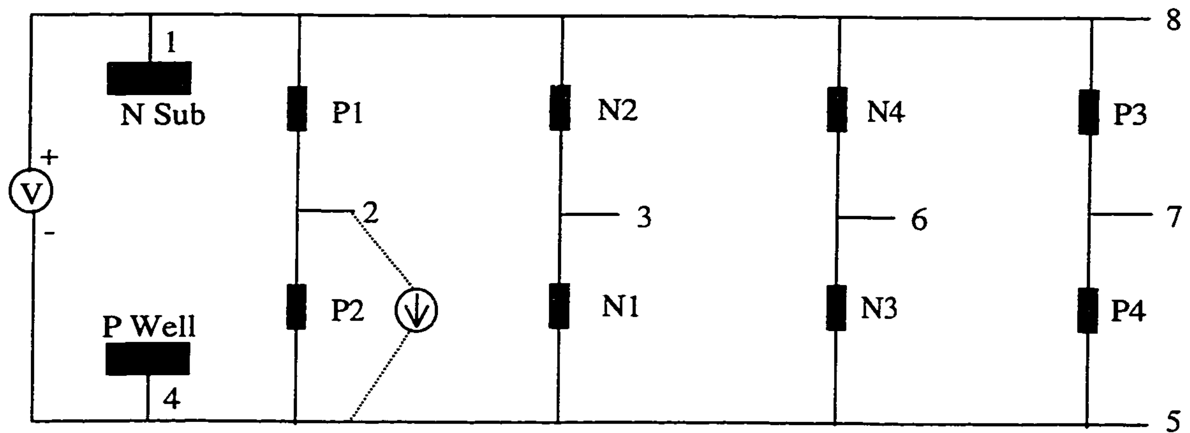
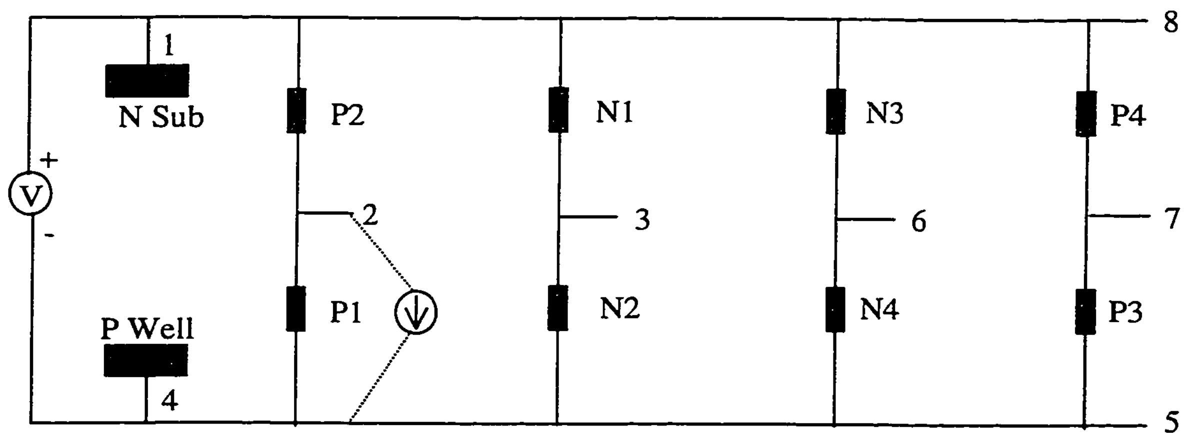


Wiring to Evaluate Sensor P1 in a Horizontal (Type 1) Rosette



Wiring to Evaluate Sensor P2 in a Vertical (Type 2) Rosette

Figure 4.16 - Typical Resistance Measurement Wiring Diagram for

the BMW-2 Test Chip Rosette

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	Channel Status	
Pad Number	H	L
1, 8	1	
2	2	3
3	5	6
4, 5		4
6	7	8
7	9	10

Table 4.5 - Connection between Bonding Pads and Channels in

a Bank of One Scanner Card

connection at the top of the half-bridge resistors as indicated in Fig. 4.17. The output voltages at the nodes V_I ... V_4 are then proportional to the four normalized resistance change difference terms present in the expressions in Eq. (4.4, 4.5). For example, V_I is proportional to

$$V_1 \propto \left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3} \right) \tag{4.9}$$

for small fractional resistance variations.

In this particular work, however, the individual resistor changes were measured directly utilizing the techniques shown in Figure 4.18 and described above. For the case in Figure 4.18, an ammeter is used to force the current in upper resistor R_U to bypass lower resistor R_L and flow through the ammeter. The ammeter must force the voltage

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across R_L to be zero and should be implemented using a high quality electrometer (such as the Keithley 6512 described above). The circuit in Figure 4.19 functions in a similar manner. In this case the ammeter forces the current in resistor R_U to be zero, and the measured current is due to resistor R_L acting alone.

Wiring diagrams for the AAA-2, BMW-1, and BMW-2 resistance measurements viewed as chip cross-sections are presented in Appendix B.

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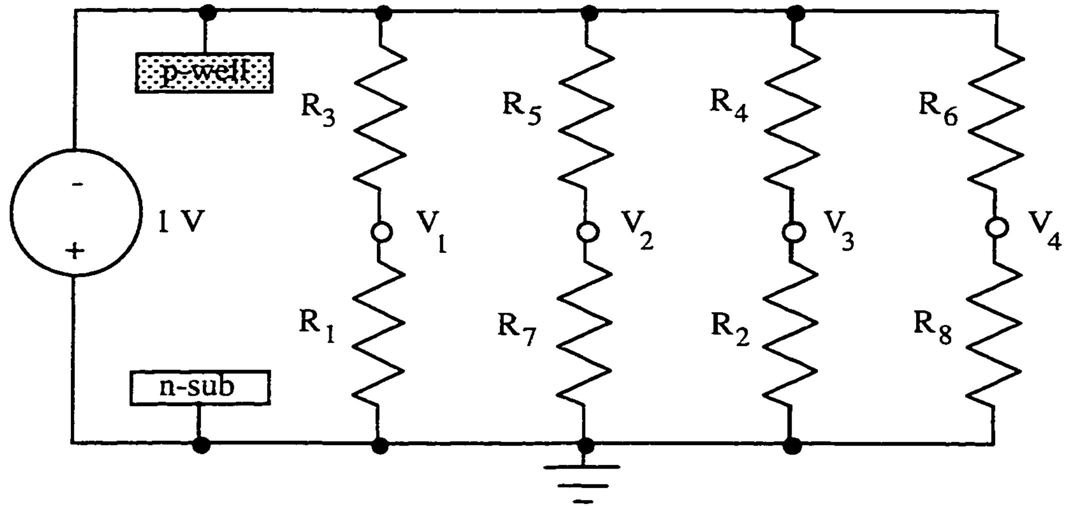

Figure 4.17 - Bias for Resistance Measurements of BMW-2 Sensor Rosette

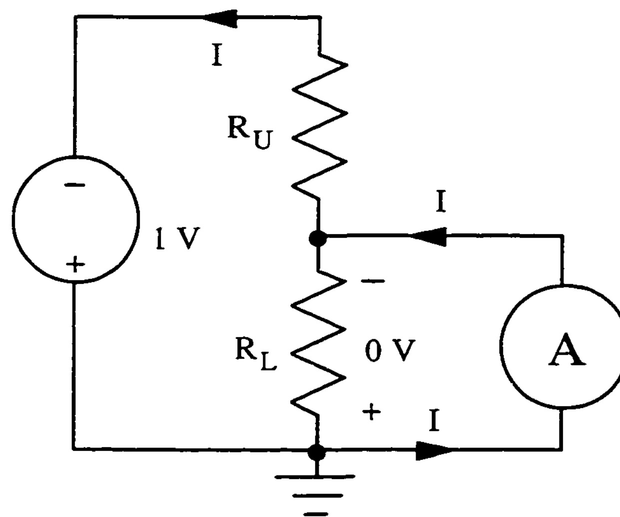

Figure 4.18 - Bias for Resistance Measurements

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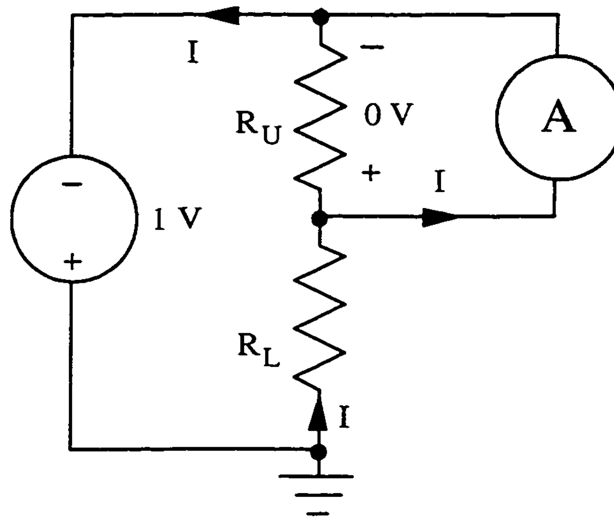

Figure 4.19 - Bias for Resistance Measurements

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CHAPTER 5

CHARACTERIZATION OF PLASTIC PACKAGES

5.1 Introduction

Plastic packages continue to play an important role in the area of microelectronics because of the cost and reliability considerations. Plastic packages are now found in military applications because the characteristics of plastic molding compounds have improved. The plastic molding compound encapsulates the chips for protection during package assembly, shields the chips from corrosive environmental contaminants, and dissipates generated heat. On the other hand, various reliability issues are introduced with the application of plastic molding compounds. High thermal stresses can be induced after packaging and during temperature cycling due to the mismatch of coefficients of thermal expansion (CTE) of the various materials. Moisture related corrosion can also occur due to moisture penetration of the molding compound and delaminations at the interfaces with other materials. Such delaminations can be caused by poor interfacial adhesion between the molding compound and other packaging materials. Reliability issues related to postmolded IC packages have been reviewed by Nuguyen [3].

It is becoming more desirable to characterize the stress levels in plastic packages and to optimize package design by considering several molding compounds. Some researchers have put efforts into characterizing plastic packages using piezoresistive stress

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test chips [6, 8, 36, 93, 97]. In this study, Auburn AAA-2 (100) silicon test chips have been encapsulated in 44 pin PlasticLeaded Chip Carrier (PLCC) packages. Several molding compounds were considered to compare the different stress levels caused by various encapsulants. Results for temperature compensated stress components σ'_{12} and $\sigma'_{11}-\sigma'_{22}$ are presented. In a related study, Auburn BMW-2 (111) silicon test chips were encapsulated in 160 pin Quad Flat Pack (QFP) packages. Two molding compounds were considered and four temperature compensated stress components were extracted including the two out-of-plane shear stresses. The stresses calculated were σ'_{12}, $\sigma'_{11}-\sigma'_{22}$, σ'_{13}, σ'_{23}. In both the AAA-2 and BMW-2 test chip applications, the room temperature resistances of the sensors were recorded before and after packaging. Stresses due to the encapsulation process were then calculated using the resistance changes and the appropriate theoretical equations. The experimental results were also correlated with the predictions of three-dimensional nonlinear finite element simulations of the package.

5.2 44 Pin PLCC Packages – (100) AAA-2 Test Chips

5.2.1 Packaging Studies

For the experiments, 100 x 100 mil AAA-2 test chips were encapsulated within 44 pin PLCC packages. Before packaging, the initial room temperature resistances of all the sensors on the test die were recorded using an automated probe station. The characterized test chips were then attached to lead frame. Fine gold wires were used to provide the interconnections from the die bond pads to the lead frame. Figure 5.1 shows a 44 pin PLCC package and several test chips attached to lead frame strip. Figure 5.2 shows the

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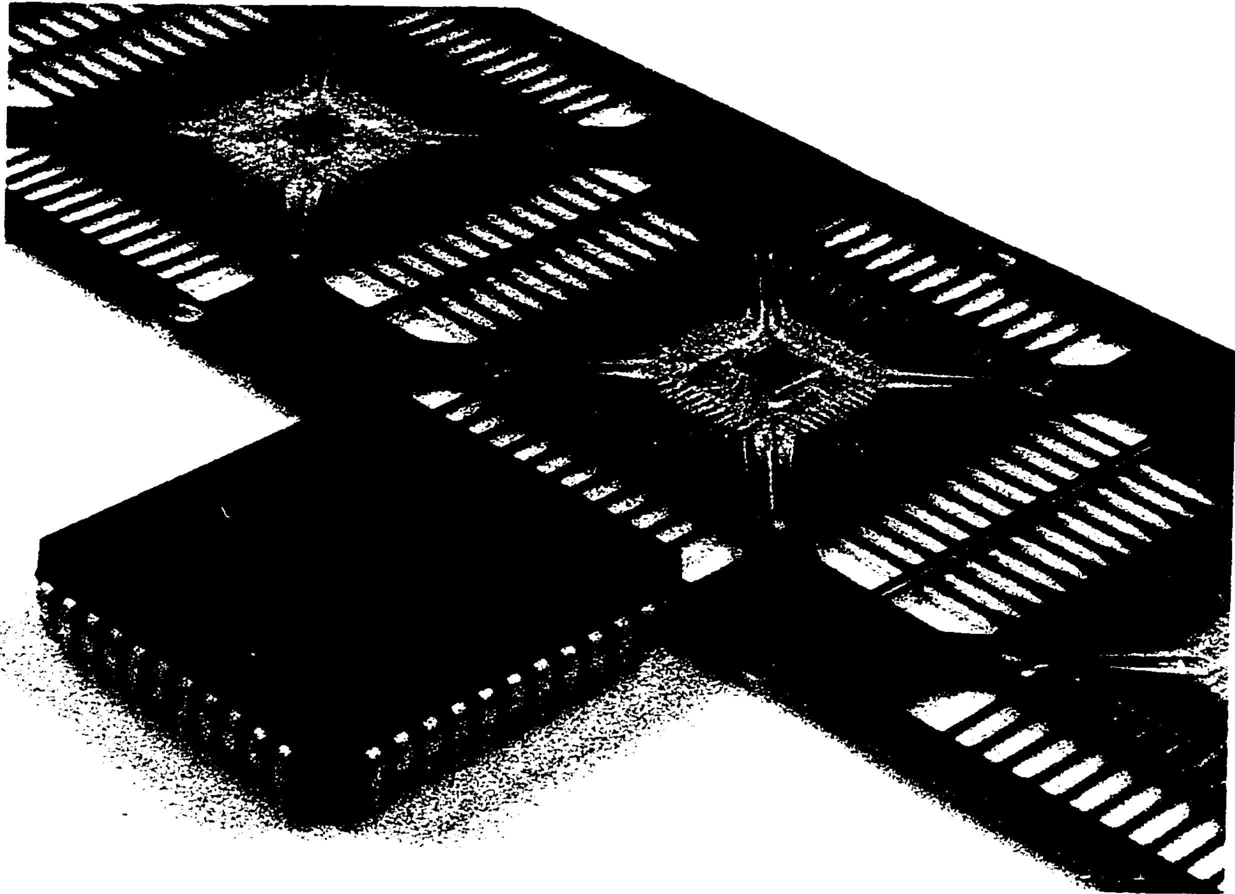

Figure 5.1 - PLCC Package and Lead Frame Strip with Test Die

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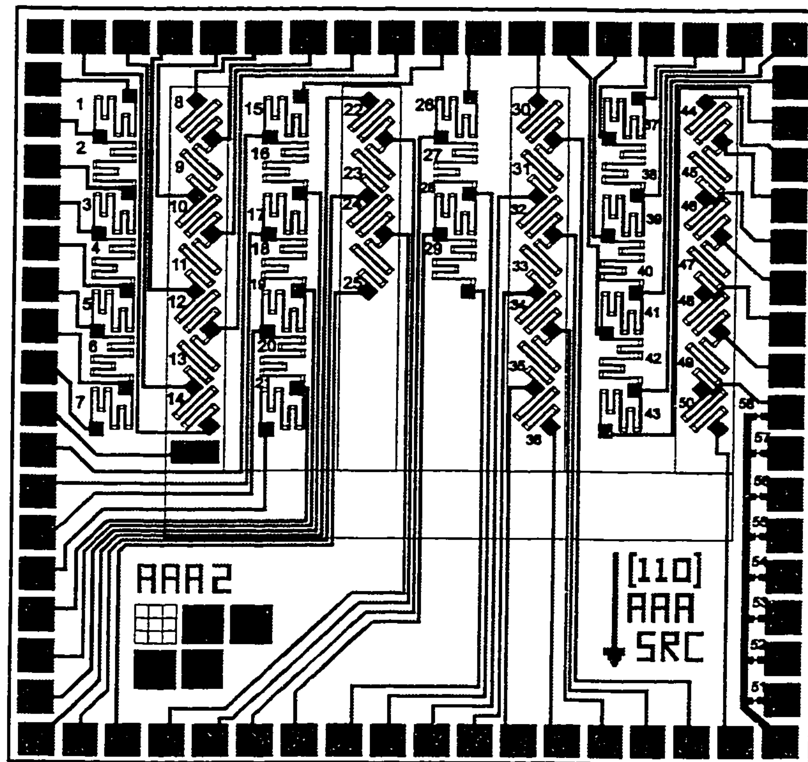

Figure 5.2 - 100 x 100 mil Test Chip

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utilized 100 x 100 mil test chip (sub-image of the chip in Figure 4.1). The selected rosette sites for stress measurement are shown in Figure 5.3. Not all of the sensors could be accessed because of the limited pin counts of the PLCC package.

Three different molding compounds were used for the purpose of studying their effects on the packaging induced stress. The modulus of elasticity E, coefficient of thermal expansion α, and glass transition temperature T_g of these mold compounds are listed in Table 5.1. These molding compounds have been referred as low stress (Compound A), medium stress (Compound B), and high stress (Compound C) according to the relative values of the properties and their influence on the packaging induced stress (the product $E*\alpha$ of the mold compound gives a rough indication of the magnitude of the induced die stresses). After encapsulation, the "post packaging" room temperature resistances of the sensors were recorded. The in-plane shear stresses and in-plane normal stresses difference were then calculated using the measured resistance changes and the theoretical expressions given in Eq. (4.2). For the AAA-2 test chip rosettes, values of $\pi_{44}^{p} = 1107$ (1/TPa) and $\pi_{D}^{n} = -850$ (1/TPa) were utilized in the equations.

Molding Compound	E (GPa)	α (ppm/°C)	T_g (°C)
A	11.0	14.0	155
B	11.7	16.5	165
C	13.8	24.0	164

Table 5.1 – Molding Compound Properties (44 Pin PLCC)

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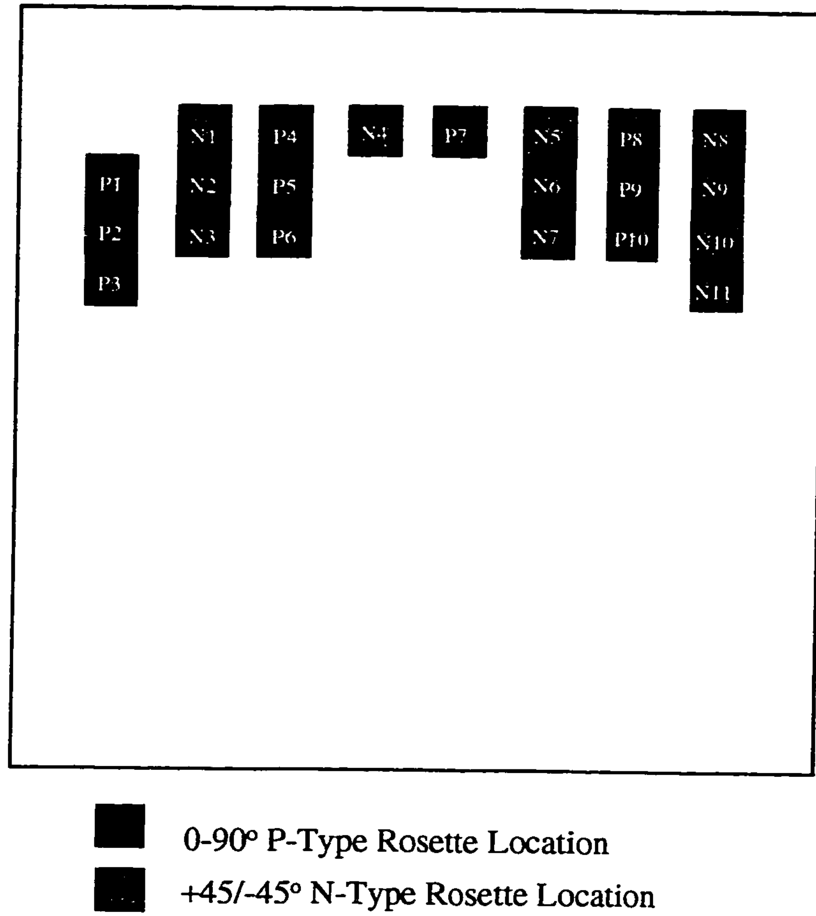

Figure 5.3 - Sensor Rosette Locations (44 Pin PLCC)

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5.2.2 Experimental Results and Comparison with FEM Predictions

The experimental results were evaluated through correlation with the predictions of nonlinear three-dimensional finite element simulations of the packaging process. In the finite element models, all materials were molded as being linear elastic. Large deformations (kinematic nonlinearities) were utilized. The time dependent (viscoelastic) behavior of the molding compound was neglected to simplify the analysis and because of a lack of material characterization data needed to generate an accurate constitutive model for the encapsulant. A quarter model of the specimen volume near the chip was meshed. The FEM model and the dimension of the model is showed in Figure 5.4. The thickness of lead frame, die attachment material, and silicon die were 0.28 mm, 0.012mm, and 0.54 mm, respectively. The die was assumed to be stress free at the glass transition temperature of the filled epoxy encapsulant, and cooling from the glass transition temperature to room temperature was simulated.

Because of the limitations in the utilized constitutive model for the encapsulants, the finite element results presented here must be viewed as only approximate. However, they are useful to understand the sign and approximate magnitudes of the stress distributions, as well as the relative influences of the mold compound material properties. Figure 5.5 and Figure 5.6 illustrate the temperature compensated experimental data and finite element predictions for the die surface distributions of the in-plane shear stress (σ'_{12}), and the in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$). In these plots, the color contours are the room temperature stress distribution predicted by the finite element models. Each of

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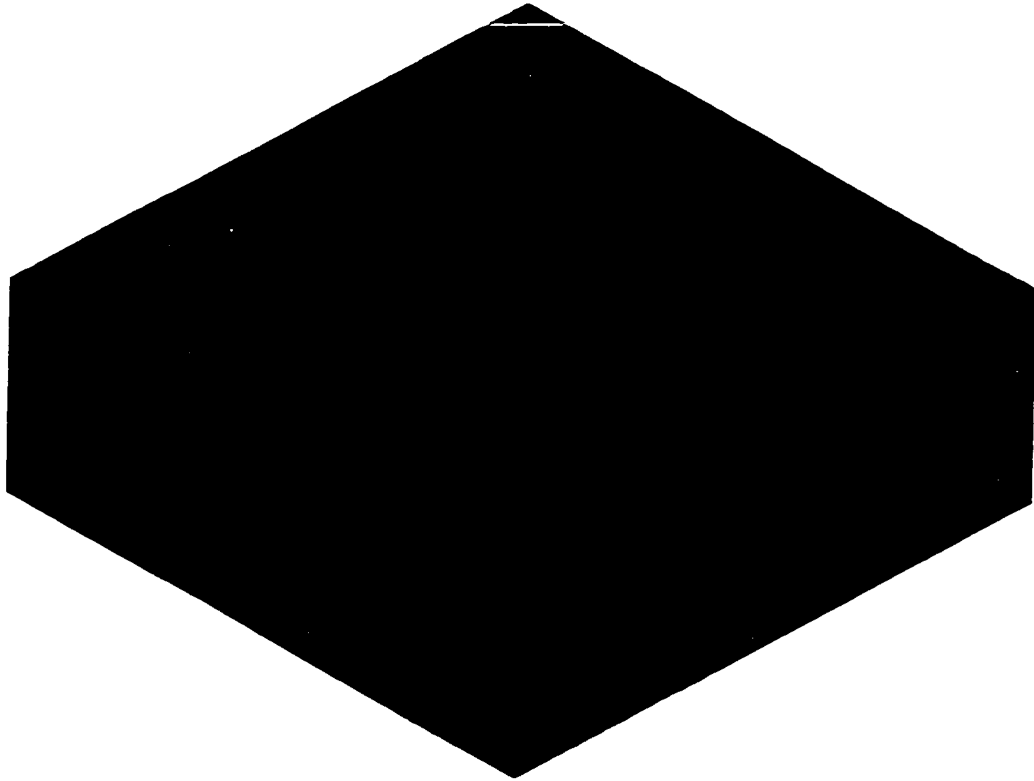

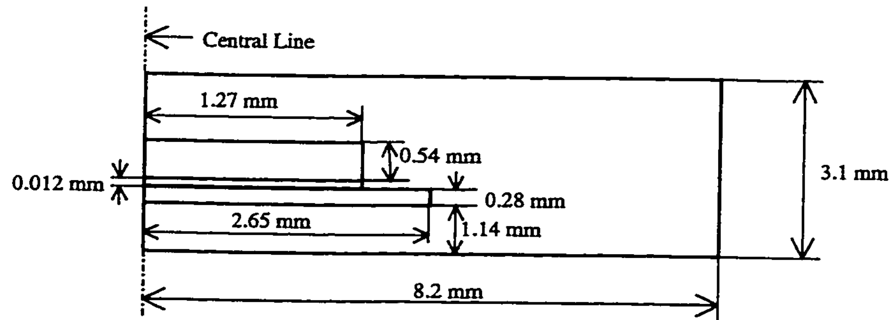

Figure 5.4 - Finite Element Mesh (One Quarter Model near the Die) and Model Dimensions (44 Pin PLCC)

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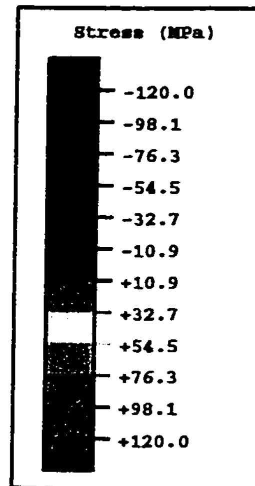
Molding Compound: A



Molding Compound: B

Molding Compound: C

Figure 5.5 - In-Plane Shear Stress Distribution Finite Element Contours and Experimental Data (44 Pin PLCC)

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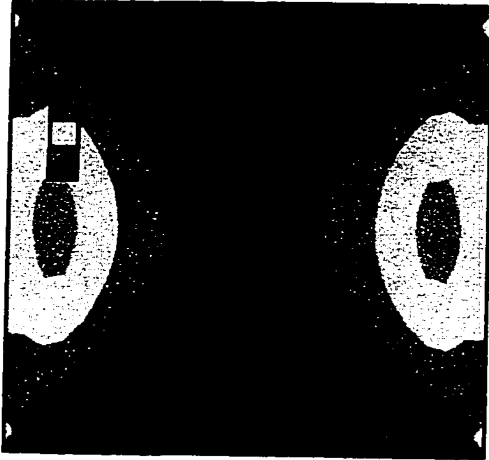
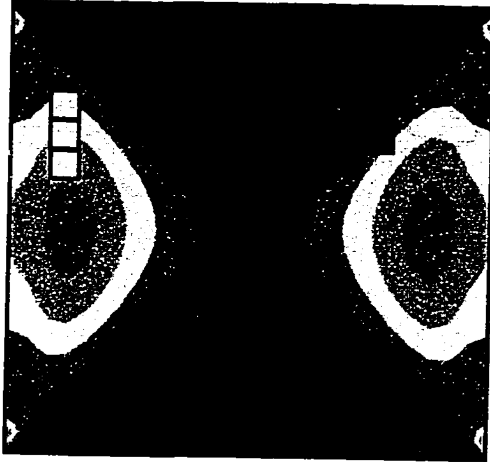
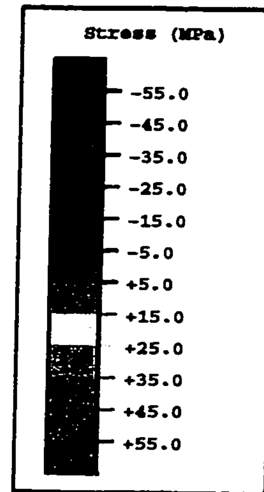
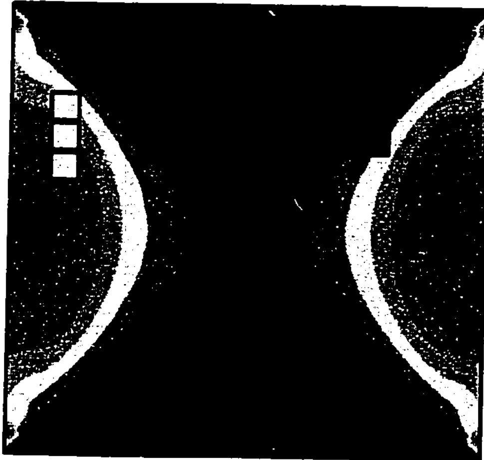


Molding Compound A



Molding Compound B





Molding Compound C

Figure 5.6 - In-Plane Normal Stress Difference Distribution Finite Element Contours and Experimental Data (44 Pin PLCC)

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the small squares in these diagrams locates a sensor rosette site and indicates its size. The color of a given square represents the average room temperature experimental value of the stress at the rosette site, when considering the results for all 10 specimens used for each mold compound (the square is colored to the same scale/legend of the finite element contours). It can be see that the finite element predictions are in reasonable agreements with the experimental results. The measured stresses show the same trends and numerical signs as the distributions predicted by finite element analysis. The correlation of the experimental and numerical shear stress values is excellent. However, the finite element models over predict the observed normal stress difference data due to the fact that the viscoelastic relaxation of the filled epoxy encapsulant was neglected. This demonstrates the valuable role that test chip data can fill as a verification tool for the assumptions made in numerical modeling techniques.

5.3 160 Pin QFP Packages – (111) BMW-2 Test Chips

5.3.1 Packaging Studies

For the experiments, 400 x 400 mil BMW-2 test chips were encapsulated within 160 Pin QFP packages. Only 18 of the 20 available rosette sites (Figure 5.7) could be accessed for stress measurements due to pin count limitations. Before packaging, the initial room temperature resistances of all the sensors on the test die were recorded using an automated probe station. After molding, the sensor resistances were again recorded by using a package socket manufactured by Yamaichi (IC51-1604-845-4). The socket was soldered to a Printed Circuit Board (PCB), which was designed to provide electrical

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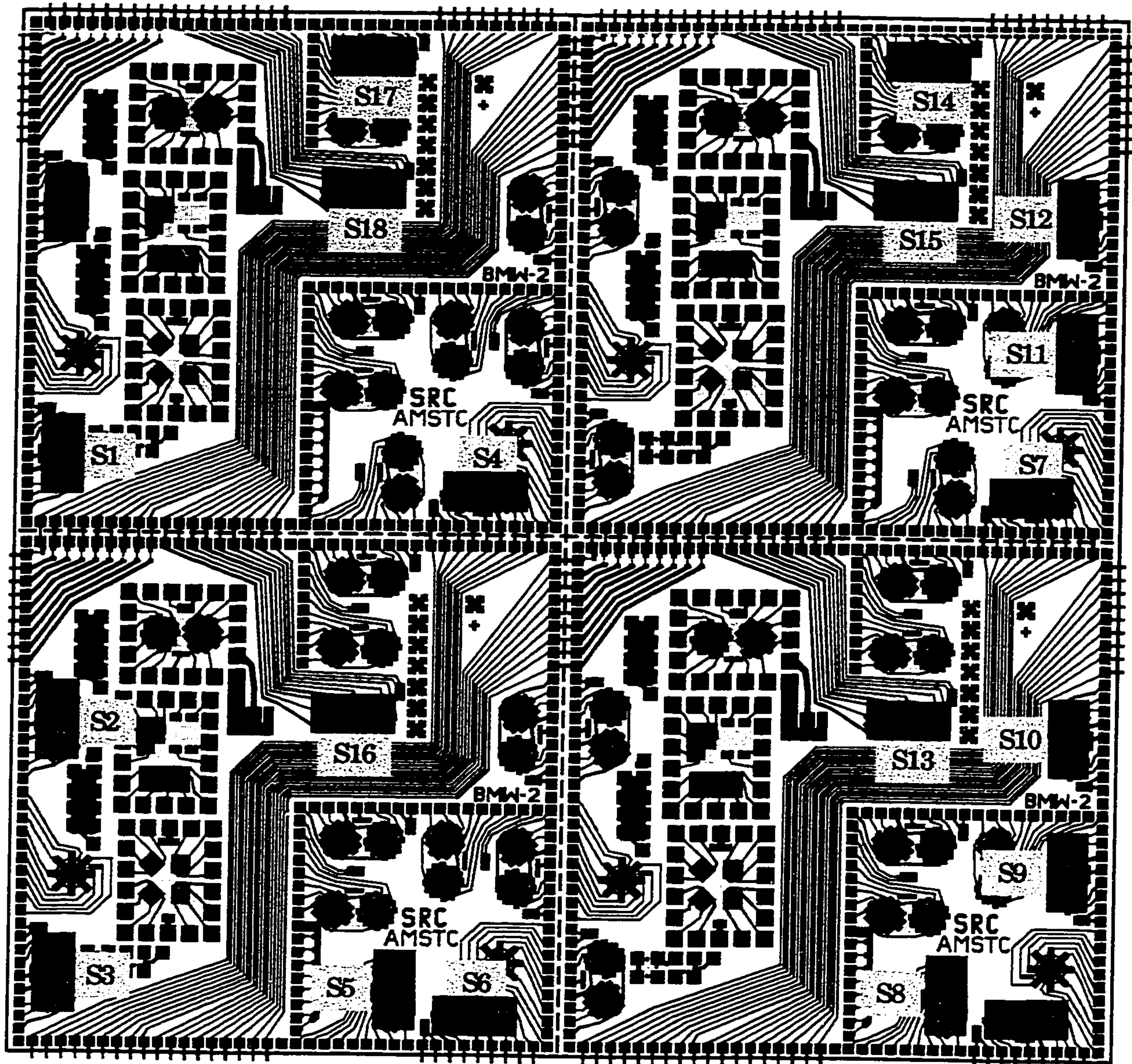

Figure 5.7 - Sensor Rosette Locations (400 x 400 mil Test Chip),
160 Pin QFP

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connections from the sensor resistors to the measurement system. The PC board was designed using Lavenir software, and the design is given in Figure 5.8. Four ribbon cable connectors were also soldered to the PC board. Using the measured resistance changes and Eqs. (4.4, 4.5), the die stresses have been calculated. The utilized BMW-2 test chips were from lot BMW2.2, and the piezoresistive coefficients were listed in Table 4.3.

A total of 108 BMW-2 test chips were encapsulated using two different molding compounds. Table 5.2 listed the modulus of elasticity E, coefficient of thermal expansion α, and glass transition temperature T_g of these materials. A total of 18 chips were encapsulated with molding compound A, and 90 chips were encapsulated with molding compound B. Compared to the previous stress calculations in 44 pin PLCC packages, two more temperature compensated stress components (out of plane shear stresses σ'_{13}, and σ'_{23}) were extracted in addition to the in-plane shear stress (σ'_{12}) and in-plane normal stresses difference ($\sigma'_{11} - \sigma'_{22}$).

Materials	E (GPa)	α (ppm/°C)	T_g (°C)	E* α
Compound A	18.6	11.0	160	204.6
Compound B	11.7	16.5	165	193.1
Lead Frame	132.4	17		
Die Attach	7.4	52		

Table 5.2 – Material Properties (160 Pin QFP)

5.3.2 Experimental Results and Comparison with FEM Predictions

The average stress values at the various rosette sites are presented in Figure 5.9. The stress indexes E* α and glass transition temperatures T_g of molding compounds A

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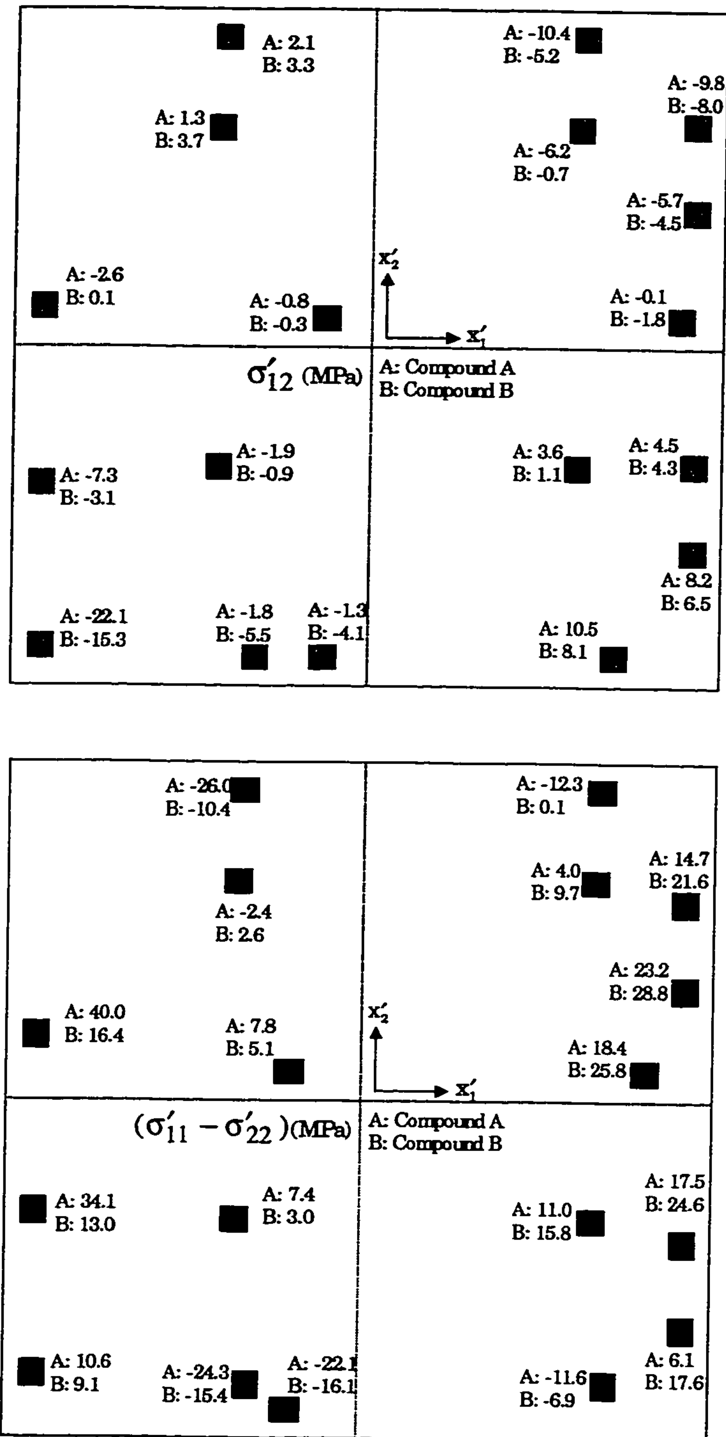

Figure 5.9 - Die Stresses After Encapsulation, 160 Pin QFP

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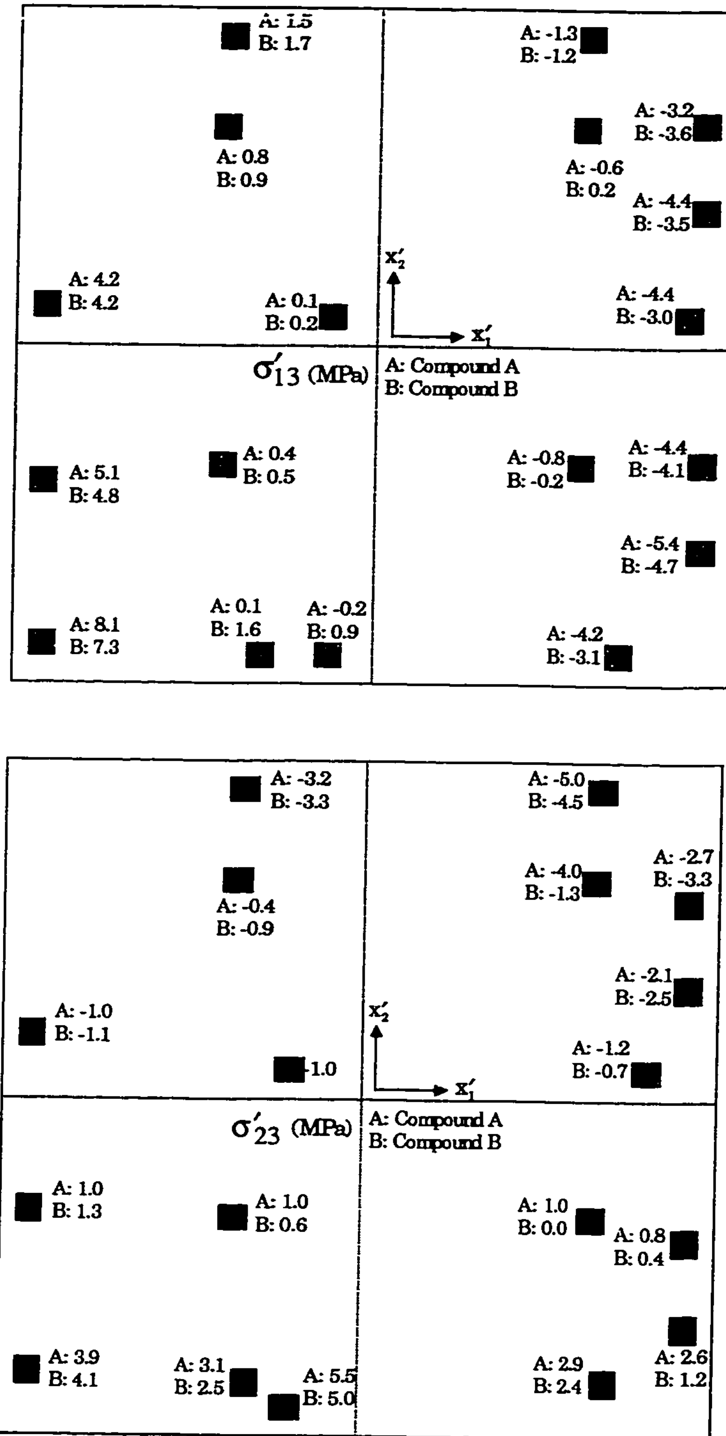

Figure 5.9 - Die Stresses After Encapsulation, 160 Pin QFP (Continued)

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and B are about the same, indicating the induced that die stresses is these two types of packages should be at about the same level. This is true for the out-of-plane shear stress components σ'_{13} and σ'_{23}, whose maximum stress magnitude is 8.1 MPa. On the other hand, the in-plane normal stress differences found with molding compound A are as much as 160% higher (at site 2) than those found with molding compound B, with some exceptions at the measurement locations on the right hand side of the silicon die. Also, the in-plane shear stresses for molding compound A are higher at most of the measurement sites (40% higher at site 3) than those for molding compound B.

The measured stress component magnitudes were abnormally distributed in this study. The values of the measurement standard deviations were as high as 100% of the average values. Table 5.3 shows some measurement results with standard deviations. A reported assembly problem was that the adhesion between die and lead frame was poor in some cases, causing the die to move under wire bonding, leading to die/edge cracking. This might be the key factor that led to the large standard deviations. In addition, irregular micro-cracks in encapsulants around silicon die or the initiation of delaminations due to the thermal stresses induced by the encapsulation may contribute to such inconsistent results. Larger standard deviation numbers were observed for packages with molding compound B than those with molding compound A. This could be due to the fact that molding compound B has a lower room temperature flexural strength (93.1 MPa) than that for molding compound A (156.8 MPa). The presence of micro-cracks and delaminations could also cause stress relief.

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Stress (MPa) (Site)	$\lvert\sigma'_{11}-\sigma'_{22}\rvert$ (Site #1)	$\lvert\sigma'_{11}-\sigma'_{22}\rvert$ (Site #2)	$\lvert\sigma'_{11}-\sigma'_{22}\rvert$ (Site #7)	$\lvert\sigma'_{12}\rvert$ (Site #3)	$\lvert\sigma'_{12}\rvert$ (Site #8)	$\lvert\sigma'_{12}\rvert$ (Site #8)
Compound A Average and Standard Deviation	40.1(22.9)	34.1 (22.0)	18.4 (12.0)	22.1 (6.7)	10.5 (5.7)	10.4 (4.0)
Compound B Average and Standard Deviation	16.4(14.9)	13.0 (14.5)	25.8 (12.1)	15.3 (5.0)	8.1 (4.1)	5.2 (6.4)

Table 5.3 - Average Measured Stresses at Selected Locations with Standard Deviation (160 Pin QFP)

The experimental results were also evaluated through correlation with the predictions of nonlinear three-dimensional finite element simulations of the packaging process. In the FEM models, all materials were modeled as being isotropic and linear elastic, except for the silicon die where anisotropic material properties were used [134]. The material properties applied in the FEM modeling were also listed in Table 5.2. Large deformations (kinematic nonlinearities) were utilized, and the viscoelastic behavior of the molding compound was neglected to simplify the analysis and due to a lack of material characterization data. A full model of the specimen volume was meshed. The die was assumed to be stress free at the glass transition temperature of the filled epoxy encapsulant, and cooling from the glass transition temperature to room temperature was simulated. The dimensions of the package used in the FEM modeling are showed in Figure 5.10. The lead frame was simplified as a single copper pad with a thickness of 0.19 mm. The thicknesses of the die and die attachment layer were 0.47 mm and 0.06 mm, respectively.

Figures 5.11 - 5.14 illustrate the temperature compensated experimental data and finite element predictions for the die surface distributions of the in-plane shear stress (σ'_{12}),

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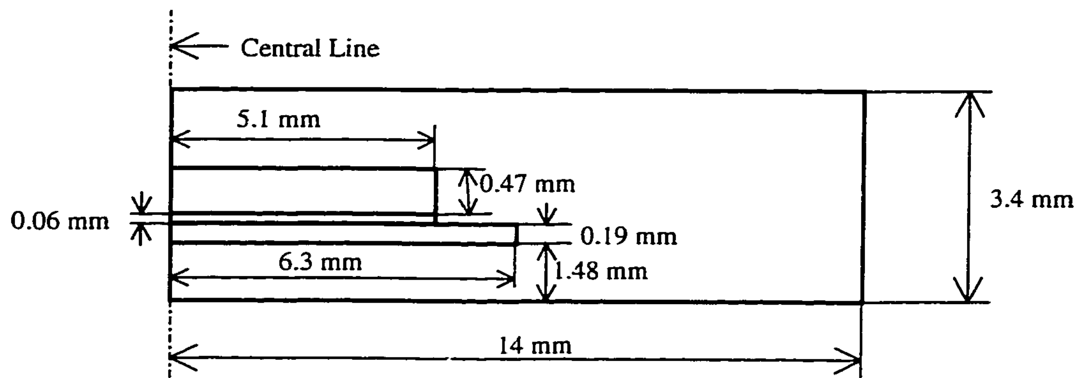

Figure 5.10 - Cross Section of a half 160 Pin QFP for FEM Simulation

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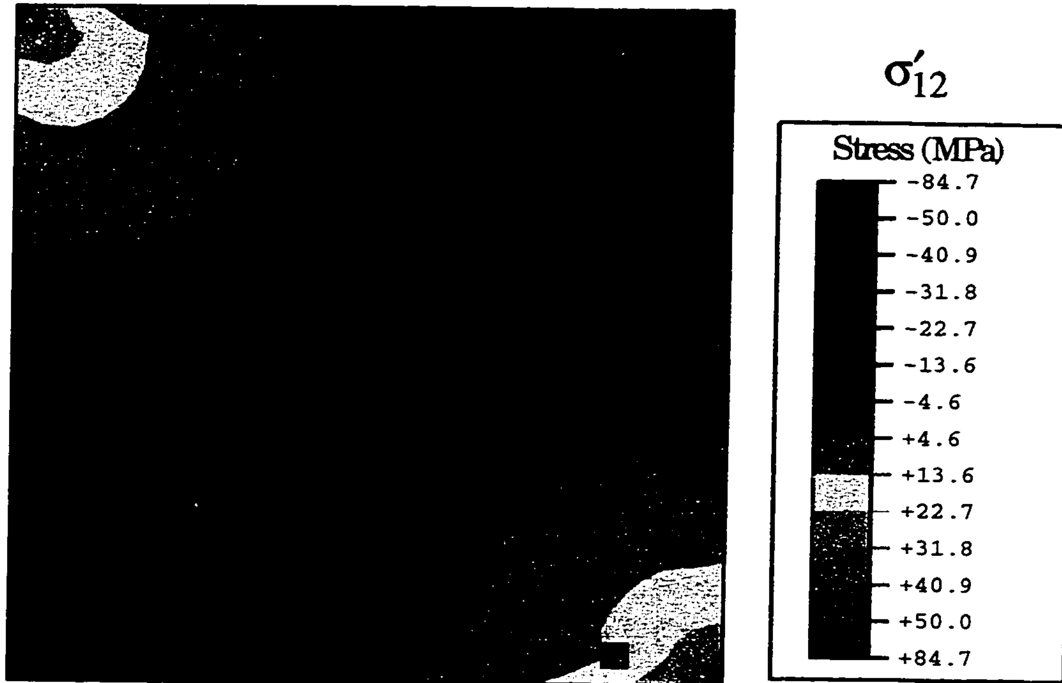
Molding Compound A



Molding Compound B

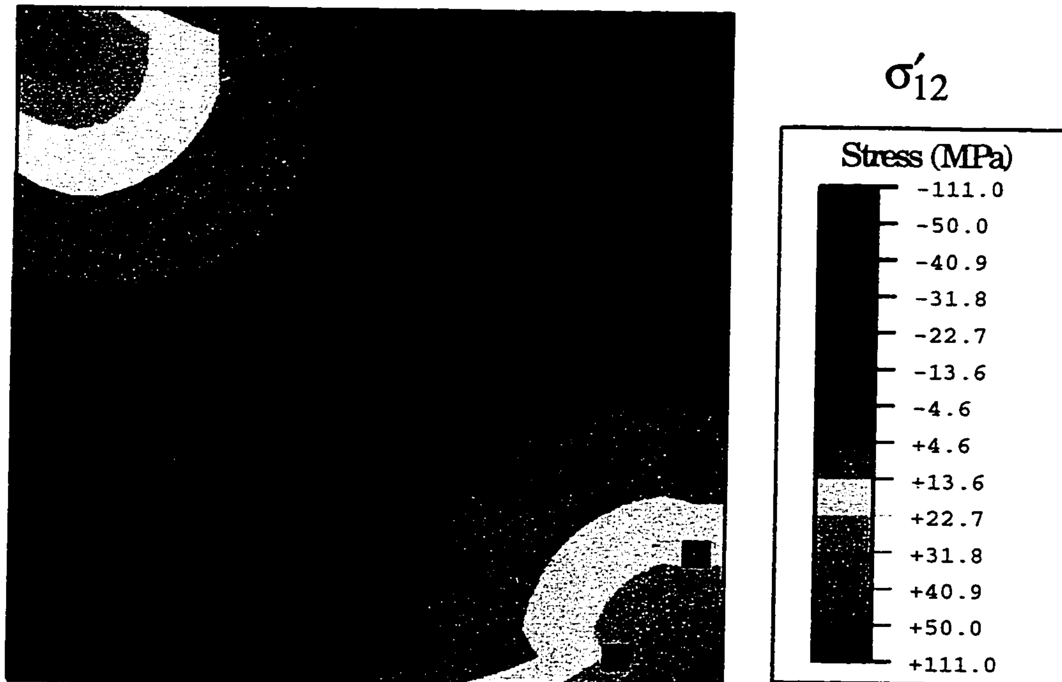


Figure 5.11 - In-Plane Shear Stress Distribution
Finite Element Contours and Experimental Data (160 Pin QFP)

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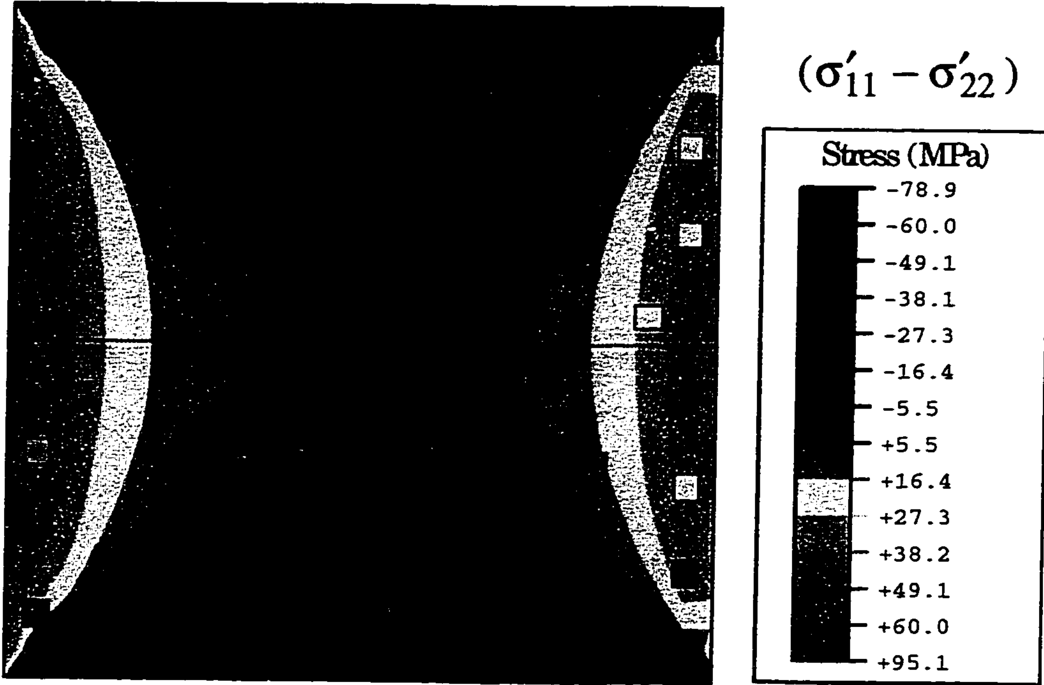
Molding Compound A



Molding Compound B

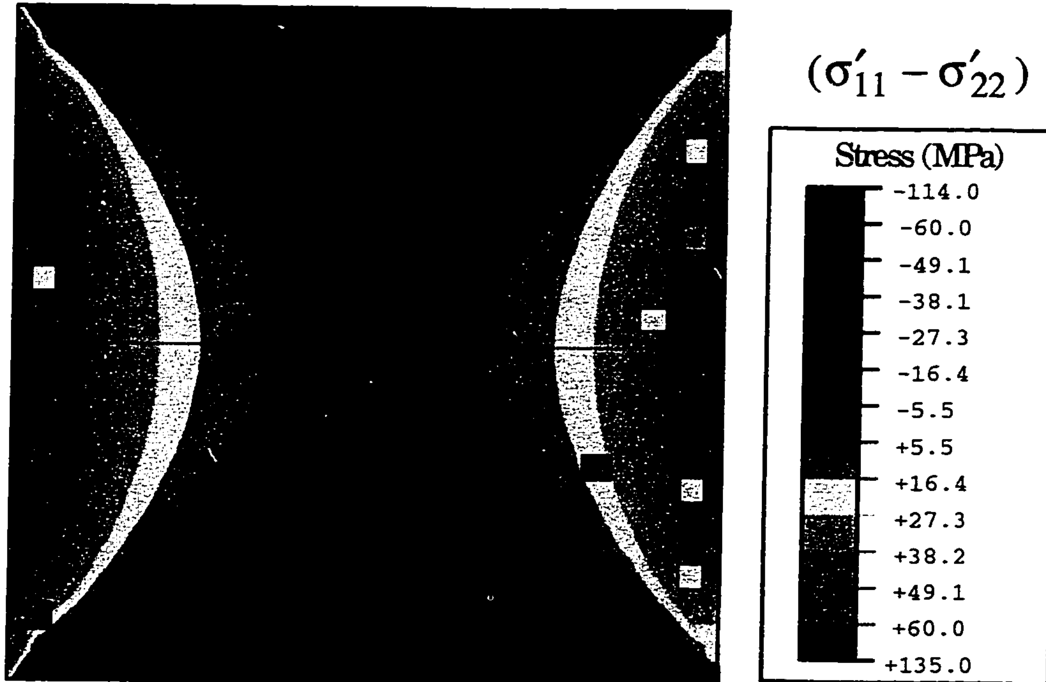


Figure 5.12 - In-Plane Normal Stress Difference Distribution
Finite Element Contours and Experimental Data (160 Pin QFP)

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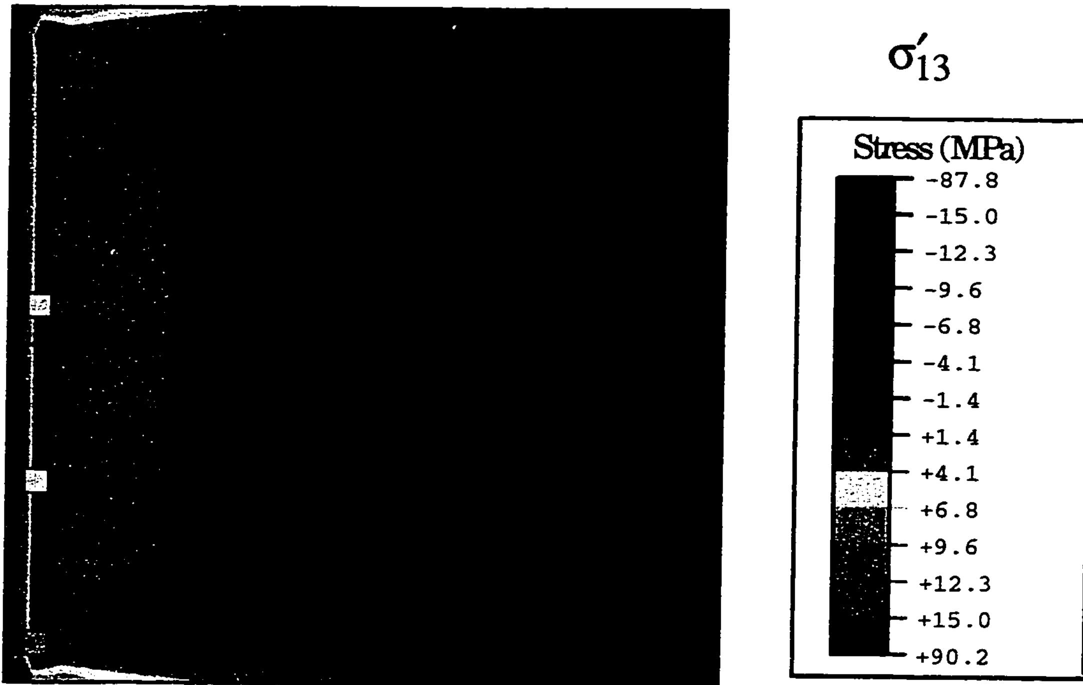
Molding Compound A



Molding Compound B

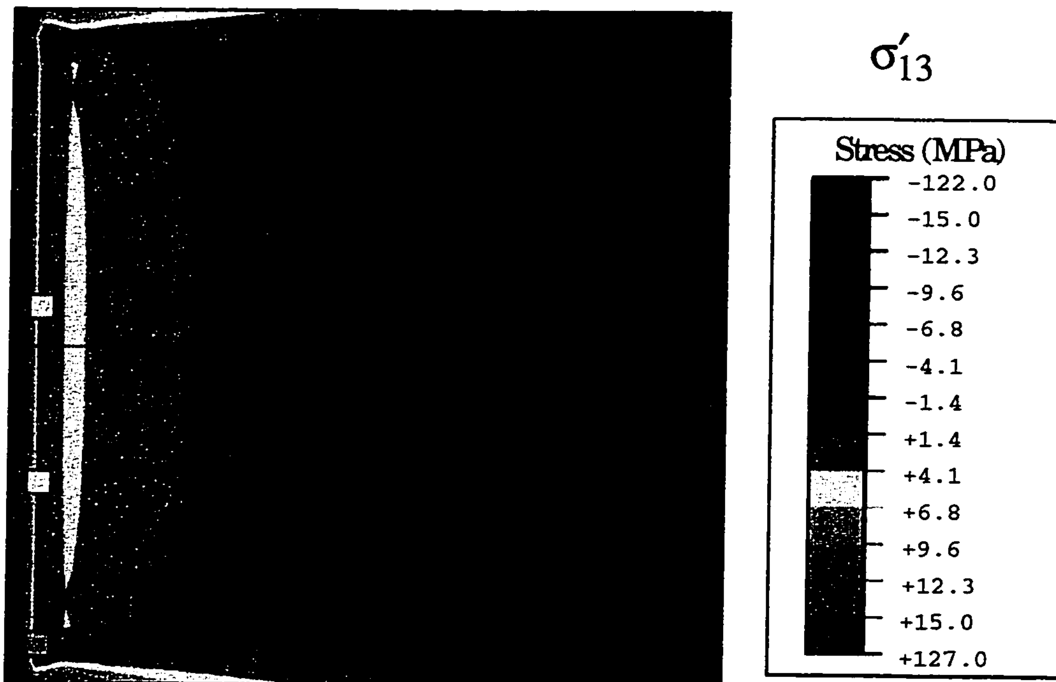


Figure 5.13 - Out-of-Plane Shear Stress σ'_{13} Distribution
Finite Element Contours and Experimental Data (160 Pin QFP)

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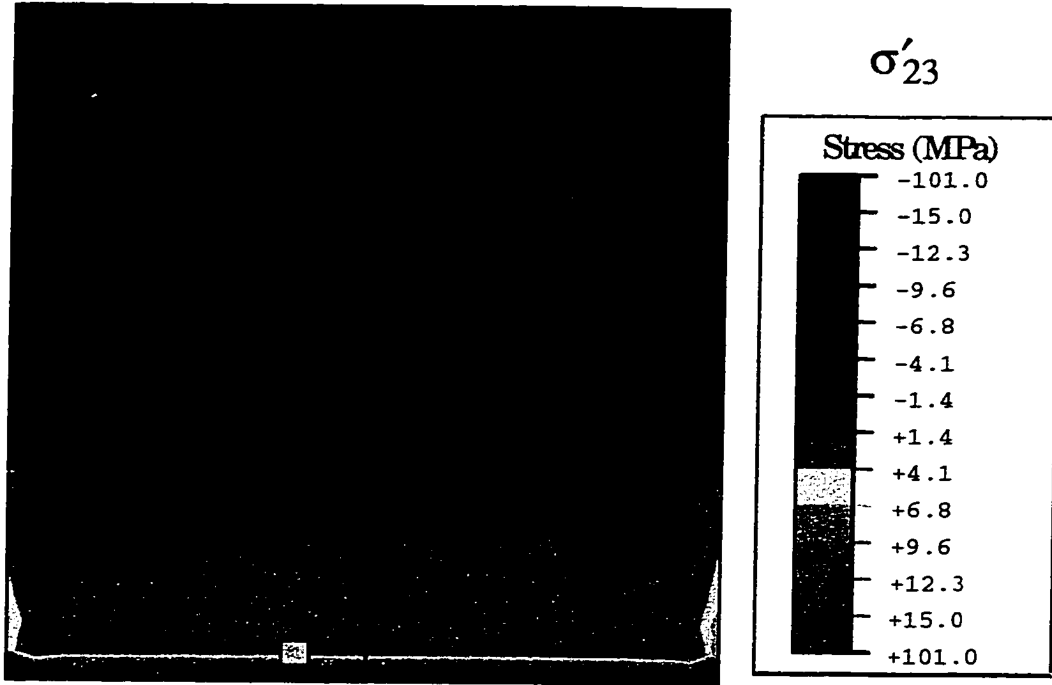
Molding Compound A



Molding Compound B

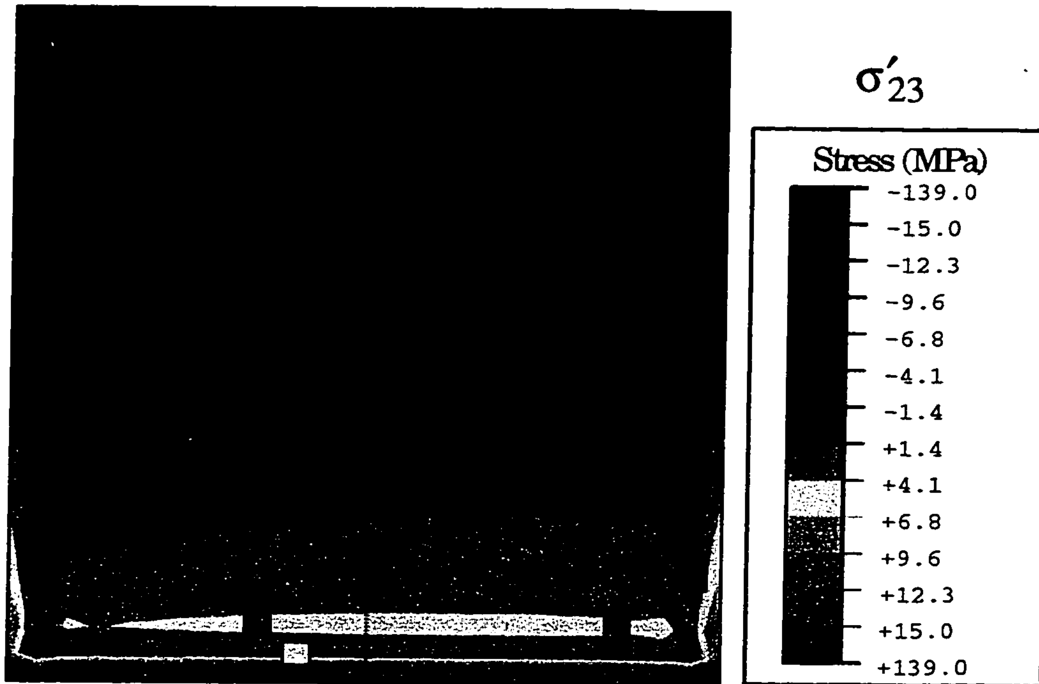


Figure 5.14 - Out-of-Plane Shear Stress σ'_{23} Distribution
Finite Element Contours and Experimental Data (160 Pin QFP)

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in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$), and out-of-plane shear stresses σ'_{13}, and σ'_{23} for molding compounds A and B. In these plots, the color contours are the room temperature stress distribution predicted by the finite element models. Each of the small squares in these diagrams locates a sensor rosette site and indicates its size. The color of a given square represents the average room temperature experimental value of the stress at the rosette site, when considering the results for all the specimens used for each mold compound (the square is colored to the same scale/legend of the finite element contours).

It can be see that the finite element predictions are in reasonable agreements with the experimental results, especially for the package samples with molding compound A. The measured stresses show the same trends and numerical signs as the distributions predicted by finite element analysis. The correlation of the experimental and numerical shear stress values is good. However, the finite element model over predicts the observed normal stress difference data due to the fact that the viscoelastic relaxation of the filled epoxy encapsulants was neglected. Furthermore, the FEM models assumed perfect bonds at the interfaces of various materials, and allowed for no relative sliding along interfaces. This is potentially a poor assumption at the edges or the corners of the silicon die, where large in-plane or out-of-plane shear stresses occur. Plastic deformations or micro-cracks in the epoxy molding compound near the edges of the silicon die could also be blamed for the lower stress magnitudes observed in the experiments. As stated previously, more micro-cracks or delaminations may have happened in the samples with molding compound B. Therefore, this could have led to poorer comparisons between the experimental data and the FEM predictions.

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5.4 Summary

In this chapter, both (100) and (111) silicon test chips containing an array of piezoresistive stress sensor rosettes have been applied within plastic encapsulated electronic packaging configurations. Calibrated and characterized (100) test chips (100 x 100 mil) were packaged in 44 pin PLCC packages using three molding compounds referred as low, medium, and high stress, and the stresses were evaluated from the post packaging room temperature sensor resistances. A set of (111) silicon test chips (400 x 400 mil) were packaged in 160 pin QFP packages with two molding compounds, and the stresses were also extracted from the post packaging room temperature sensor resistances. The experimental data were correlated with three-dimensional nonlinear finite element simulations of the packages. The experimental results were in reasonable agreement with the finite element predictions in most of the cases. However, improvement in the constitutive model for the filled epoxy encapsulants will further improve the finite element predictions. In the 160 pin QFP package studies, assembly problems such as poor adhesion between the die and the lead frame caused scattered experimental data. Micro-cracks in the encapsulant and delaminations at the material interfaces potentially led to stress relief in some of the samples.

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CHAPTER 6

THREE DIMENSIONAL DIE SURFACE STRESS MEASUREMENTS IN DELAMINATED AND NON-DELAMINATED 240 PIN QFP's

6.1 Introduction

One of the key reliability issues in plastic packaging is the occurrence of delaminations at the interfaces of dissimilar packaging materials. Such delaminations occur due to thermal stresses induced by packaging processes or temperature cyclic environments. Delaminations can appear at various interfaces within a plastic package, such as the interface of die surface and encapsulant, the interface of the die side walls and encapsulant, the interface of the lead frame and encapsulant, and the interface of chip pad and encapsulant, etc. The magnitudes of the interfacial thermal stresses and the adhesion strength of the interfaces are the key factors which control the occurrence of delaminations.

The damage resulting from delaminations often causes package failures. Delaminations on the die surface reduce the restriction of encapsulant movement. This can lead to metal line deformation or breaking of wire bonds. Delaminations can also serve as containers for absorbed moisture. When the packages are exposed to high temperature, the trapped moisture turns into high pressure vapor (steam) that can increase the size of the delaminations, or cause the "popcorn" phenomenon leading to package

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cracking. Damage to package integrity can also introduce electronic characteristic changes of devices or electrical failures.

The delaminations at the die/encapsulant interface are believed to occur due to the high interfacial shear stresses at the die surface. Therefore, the delaminations usually start at the corners and edges of a chip, and then proceed toward the chip center. The delaminations at interfaces of different materials can perturb the stress distributions on the die surface. Since delaminations are so unsymmetrical and variable, numerical finite element modeling becomes almost impossible.

Delamination phenomena have been studied by researchers using C-SAM techniques, reliability tests, and FEM modeling [17-22, 61]. Experimental methods can deal with delaminations qualitatively by characterizing the thermal stress fields. Numerical methods (FEM) require many assumptions that need to be verified by experimental methods. Piezoresistive stress sensors are a powerful tool to investigate stress distributions on the die surface quantitatively. Miura, et al. [36, 39] have presented research on the relation between the stress distributions and delamination areas on the die surface within a DIP package. The delaminations were generated by thermal cycling tests. The limitation of their (100) silicon test chip allowed for only in-plane shear stresses to be investigated.

In this work, (100) and (111) silicon test chips containing arrays of optimized piezoresistive stress sensor rosettes have been used to characterize die surface stresses in 240 pin Quad Flat Packs (QFP's). The sensors on the (100) test chips were able to accurately measure two in-plane stress components in a temperature compensated

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manner, while the rosettes on the (111) test chips were uniquely capable of evaluating all the 6 stress components (four in a temperature compensated manner). The results of three-dimensional nonlinear finite element simulations of the plastic encapsulated packages were correlated with the experimental data. In addition, delaminations between the die surface and the encapsulant were detected using C-Mode Scanning Acoustic Microscopy (C-SAM). The effects of the detected delaminations on the measured stress distributions were investigated, and the potential of (111) silicon stress test chips for detecting delaminations and for assisting the understanding of stress distributions in delaminated packages was explored.

6.2 Stress Measurements in Non-Delaminated Packages

6.2.1 Packaging Studies - (100) Silicon AAA2 Test Chips

For the experiments, 450 x 450 mil (3 x 3 array of the die schematic shown in Figure 4.1) AAA2 test chips were encapsulated within 240 pin QFP packages (dimensions of 1.26 x 1.26 x 0.134 inches). Before packaging, the initial room temperature resistances of all the sensors on the test die were recorded using an automated probe station. The semiconductor die was then attached to the lead frame strips using a silver filled epoxy die attachment adhesive (See Figure 6.1). Fine gold wires were used to provide the interconnections from the die bond pads to lead frame. After molding, the packages were allowed to cool down to room temperature and the sensor resistances were again recorded. Using the measured resistance changes and Eq. (4.2), the die stresses have been calculated.

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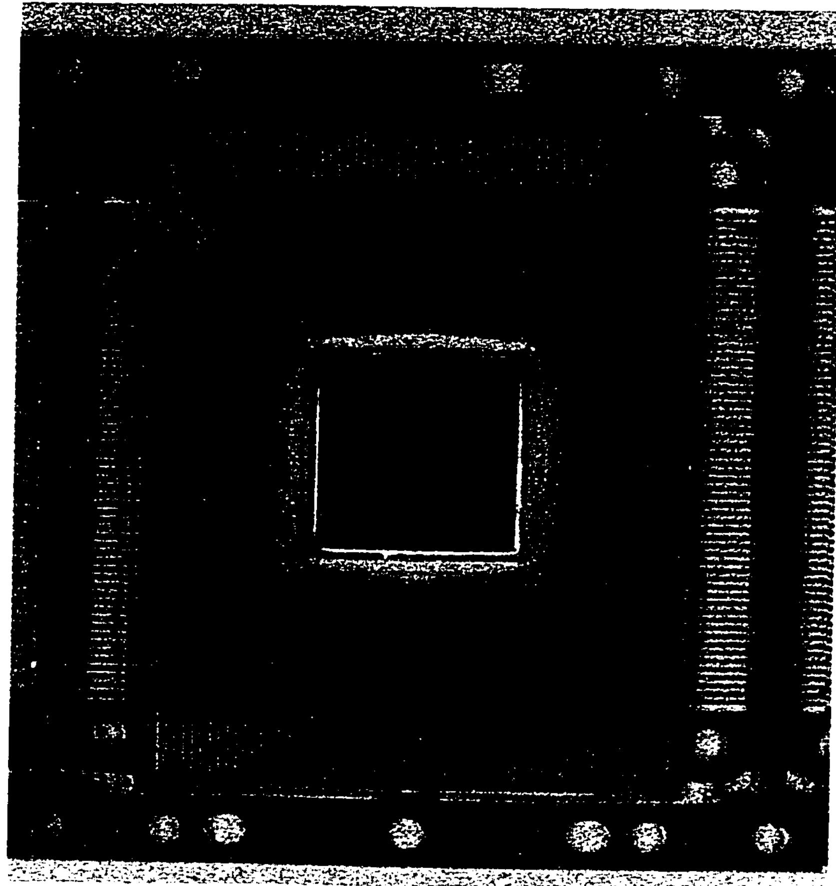

Figure 6.1 - AAA2 Test Chip Attached to Lead Frame (240 Pin QFP)

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For the AAA-2 test chip rosettes in this study, average values of π_{44}^{p}=1107 (1/TPa) and π_{D}^{n} = -850 (1/TPa) were obtained.

A total of 16 AAA-2 test chips were encapsulated. Figure 6.2 shows a typical QFP specimen (with encapsulated test chip) in the test socket used for the final resistance measurements, and Figure 6.3 shows some of the package samples with Gull wing legs. The utilized test chip and selected rosette sites for stress measurements are displayed in Figure 6.4 and Figure 6.5.

An additional four test dies were attached to lead frames but not encapsulated, so that the stresses due to only the die attachment process could be determined. After bonding, the final resistances of the die sensors were measured by directly probing the wire bond pads on the perimeter of the chip, and the stresses were then calculated from the measured resistance changes. For each of the four bonded die, the magnitudes of both the in-plane shear stresses and the in-plane normal stress differences were very small over the entire die surface. Maximum values were under 10 MPa, and typical values were in the range of 1-5 MPa. These results agree well with previously measured data for test die bonded to ceramic and FR-4 substrates [90, 97-98, 118].

The experimental encapsulation stress results were evaluated through correlation with the predictions of preliminary nonlinear three-dimensional finite element models. The materials were molded as linear elastic, but with temperature dependent material properties. Large deformations (kinematic nonlinearities) were utilized. The time dependent (viscoelastic) behavior of the molding compound was neglected to simplify the analysis and because of lack of material characterization data needed to generate an accurate

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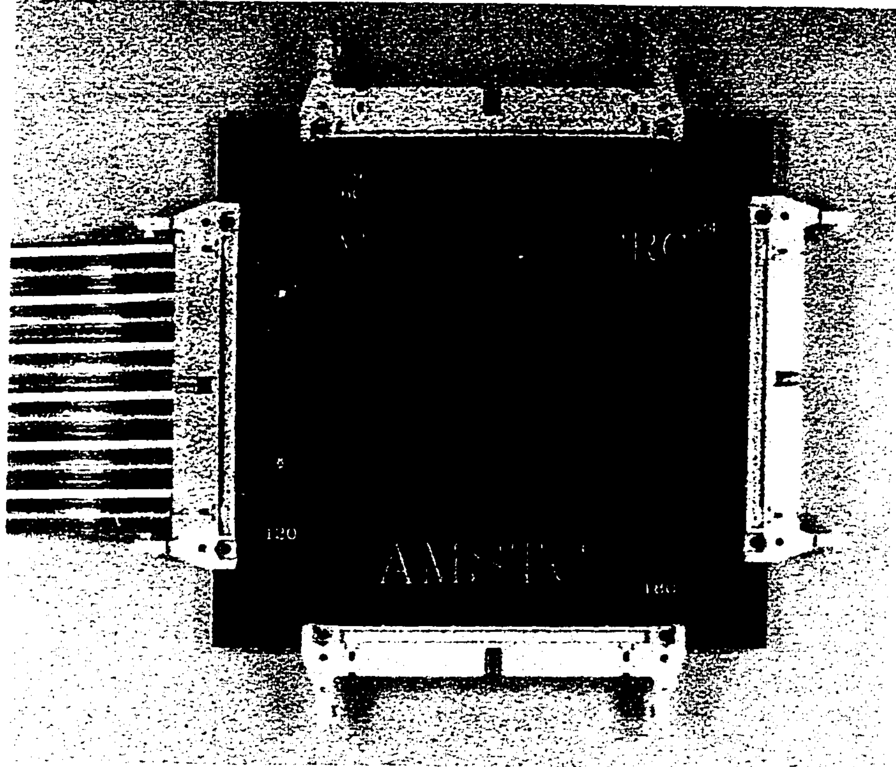

Figure 6.2 - Encapsulated Test Chip in Measurement Socket

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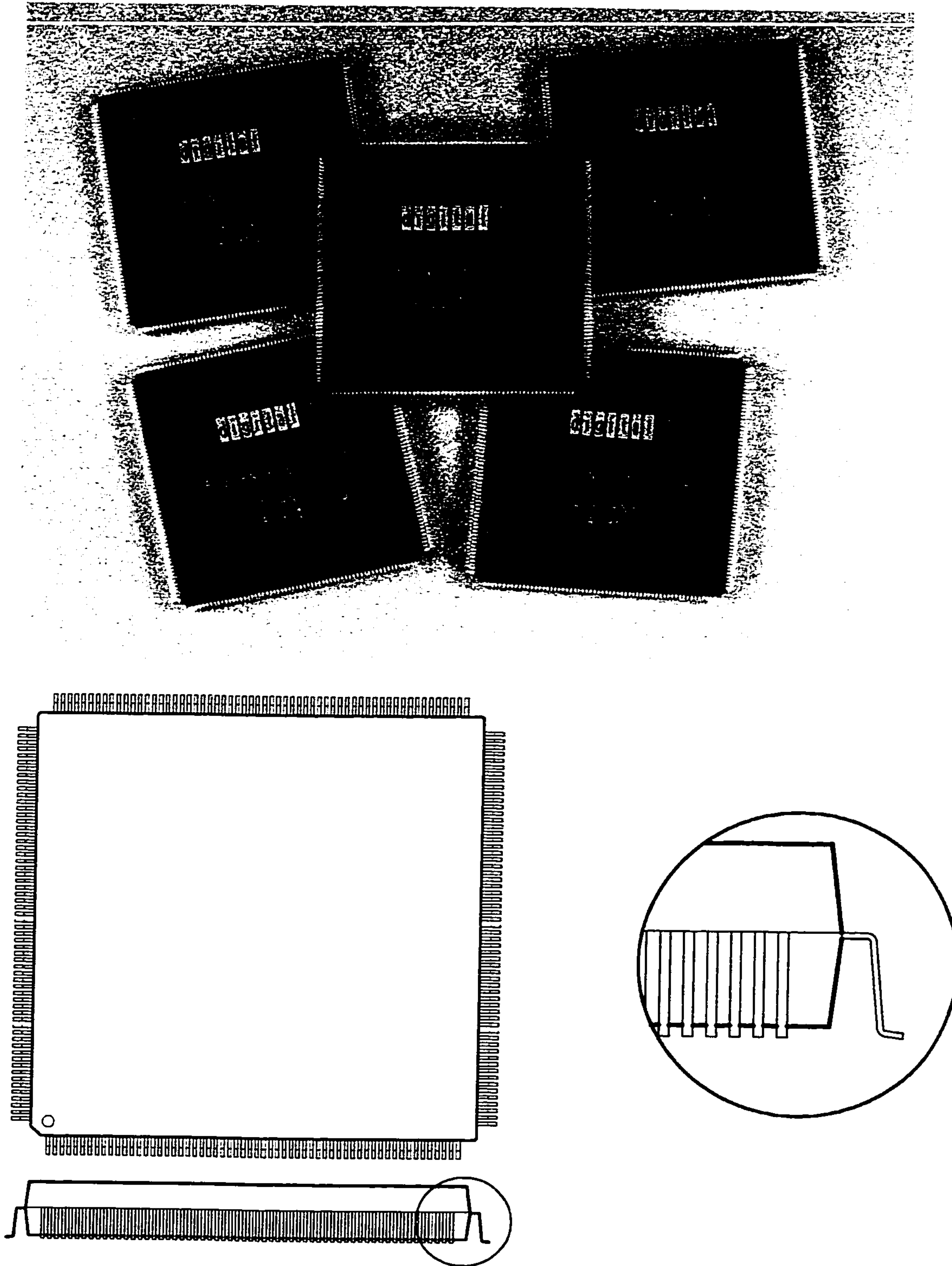

Figure 6.3 - Schematic of Packaged Die (240 Pin QFP)

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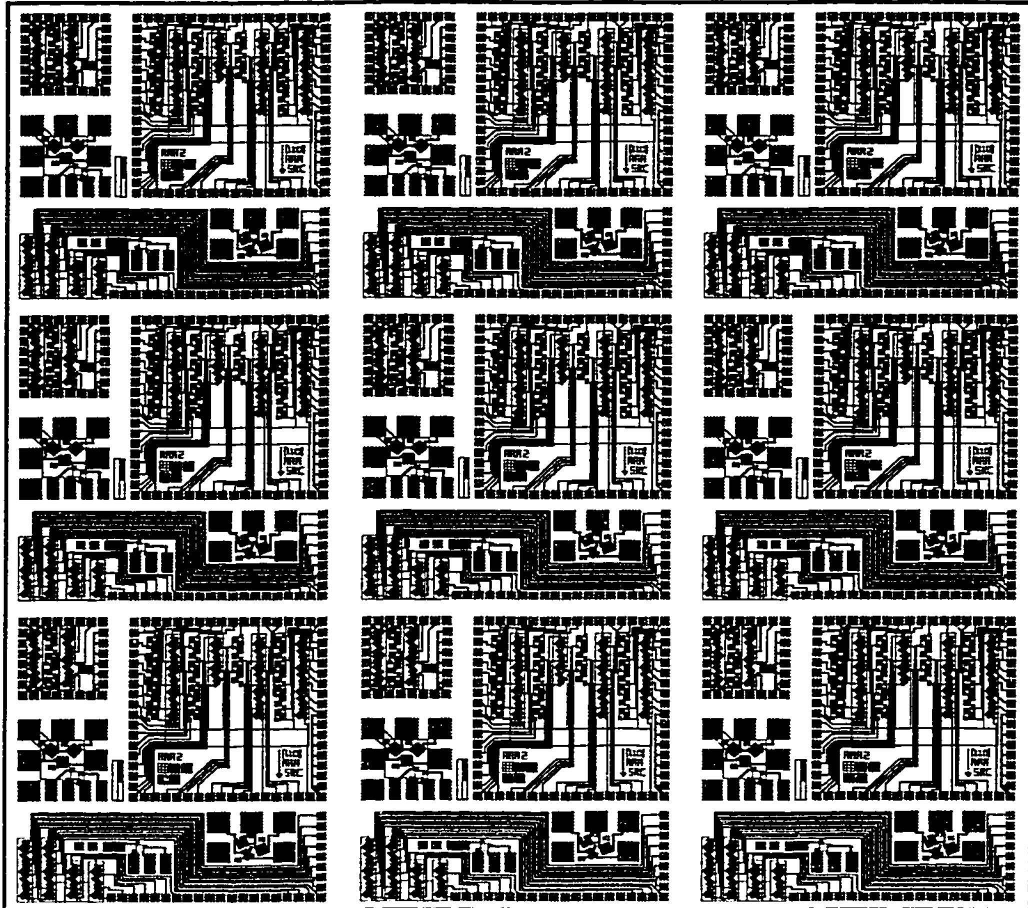

Figure 6.4 - 3x3 Array of AAA2 Test Chip

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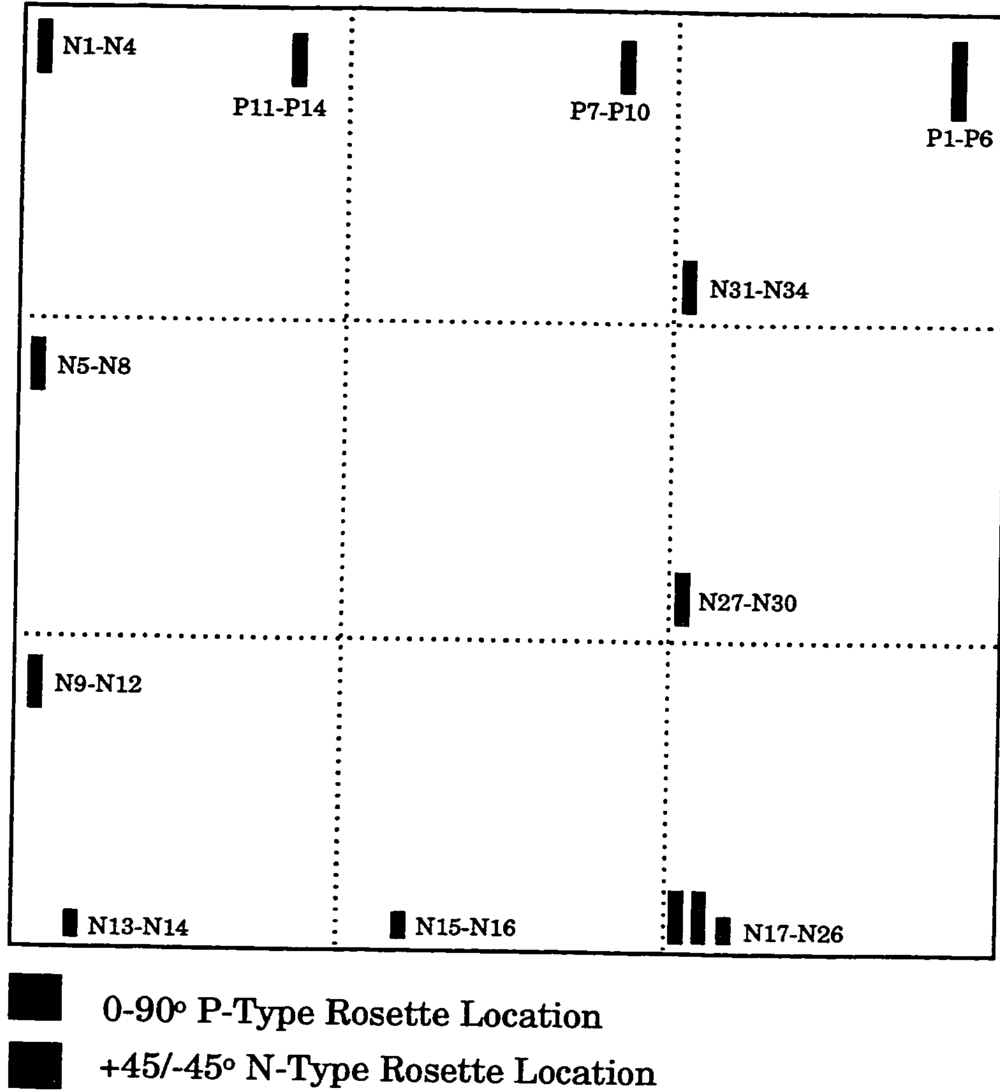

Figure 6.5 - AAA2 Sensor Rosette Locations
(450 x 450 mil Test Chip, 240 Pin QFP)

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constitutive model for the encapsulant. A quarter model of the specimen volume near the chip was meshed (see Figure 6.6). The die was assumed to be stress free at the glass transition temperature of the filled epoxy encapsulant (T_g = 155 °C), and cooling from the glass transition temperature to room temperature (25 °C) was simulated. The room temperature properties of the package materials are listed in Table 6.1.

Material	α (CTE) 1/°C	E (psi)	ν
Copper	17.0×10^{-6}	19.2×10^{6}	.34
Silicon	2.6×10^{-6}	19.0×10^{6}	.28
Epoxy	18.1×10^{-6}	1.5×10^{6}	.3

Table 6.1 - Room Temperature Isotropic Material Properties

It should be emphasized that the experimental measurements were the main emphasis of this work. The finite element model predictions were used to show the proper signs and approximate trends of the various stress component distributions, so that the experimental data could be better understood. In addition, correlation of the finite element predictions with the test chip data allowed identification of the limitations of using an expedient but approximate engineering numerical simulation procedure which neglects encapsulant relaxation.

Figure 6.7 and Figure 6.8 illustrate the temperature compensated experimental results and finite element predictions for the die surface distributions of in-plane shear stress (σ'_{12}), and the in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$). In these plots, the color contours are the room temperature stress distributions predicted by finite element model. Each of the small squares in these diagrams locates a sensor rosette site. The color of a given square represents the average room temperature experimental value of the stress at

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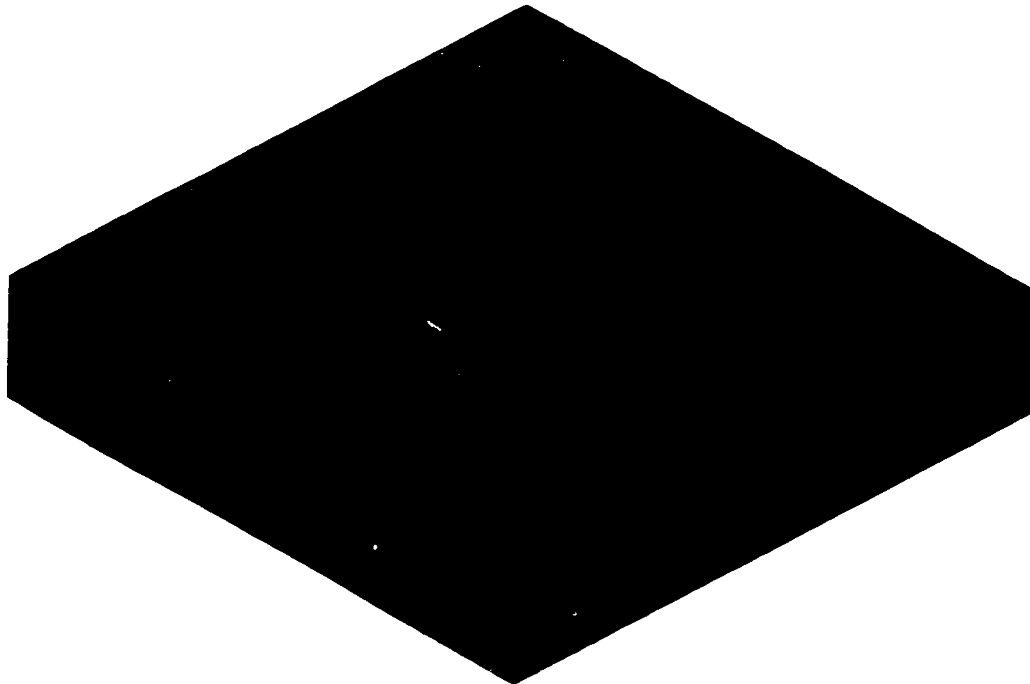

Figure 6.6 - Finite Element Mesh for the 240 Pin QFP
(One Quarter Model Near the Die)

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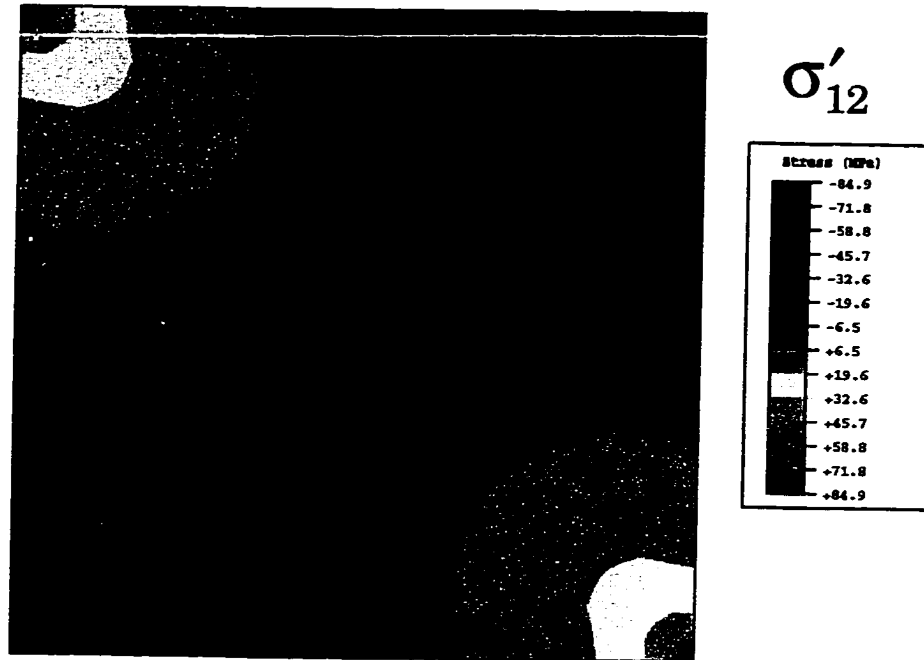

Figure 6.7 - In-Plane Shear Stress Distribution, Finite Element Contours and Experimental Data (AAA2 Chip, 240 Pin QFP)

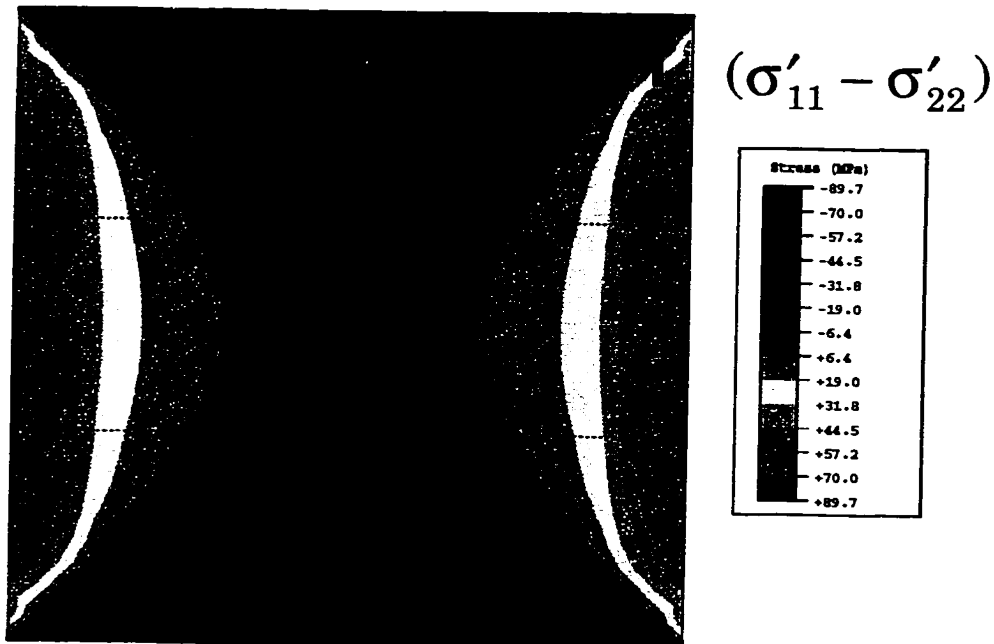

Figure 6.8 - In-plane Normal Stress Difference Distribution, Finite Element Contours and Experimental Data (AAA2 Chip, 240 Pin QFP)

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the rosette site, when considering the results for all the specimens (the square is colored to the same scale/legend of the finite element contours). It can be seen that the finite element predictions are in reasonable agreement with the experimental results. The measured stresses show the same trends and numerical signs as the distributions predicted by finite element analysis. The correlation of the experimental and numerical in-plane shear stress values is excellent. However, the finite element model over predicts the observed normal stress difference data due to the fact that that viscoelastic relaxation of the filled epoxy encapsulant was neglected. These conclusions are consistent with those obtained in other studies for different encapsulated packages [62, 81, 95, 97, 116, 117]. This also demonstrates the valuable role that test chip data can fill as a verification tool for the assumptions made in numerical modeling techniques.

C-Mode Scanning Acoustic Microscopy (C-SAM) was used to inspect the encapsulated AAA2 test chips. No delaminations were detected.

6.2.2 Packaging Studies - (111) Silicon BMW-2 Test Chips

Stress measurements in non-delaminated 240 pin QFP packages were also performed using (111) silicon BMW-2 test chips. This test chip is 2 x 2 array of the basic BMW-2 image (Figure 4.8) with dimensions of 400 x 400 mils. All 20 of the possible rosette sites were connected to the perimeter bonding pads and could be accessed for stress measurements. Figure 6.9 shows the schematic of the test die, and Figure 6.10 shows the wiring diagram. Before packaging, the initial room temperature resistances of all the sensors on the test die were recorded using an automated probe station. After the chips

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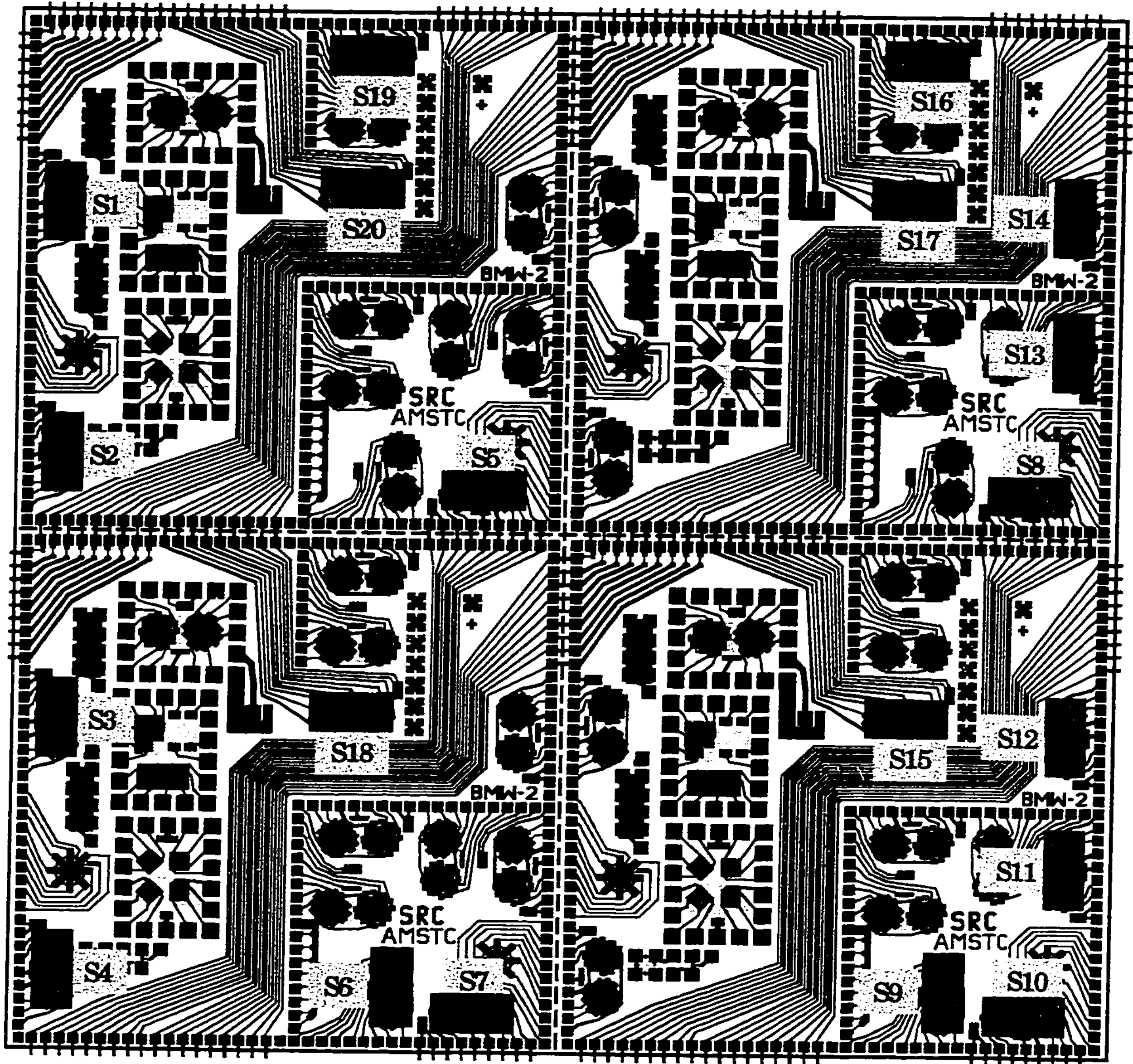

Figure 6.9 - BMW-2 Sensor Rosette Locations
(400 x 400 mil Test Chip, 240 Pin QFP)

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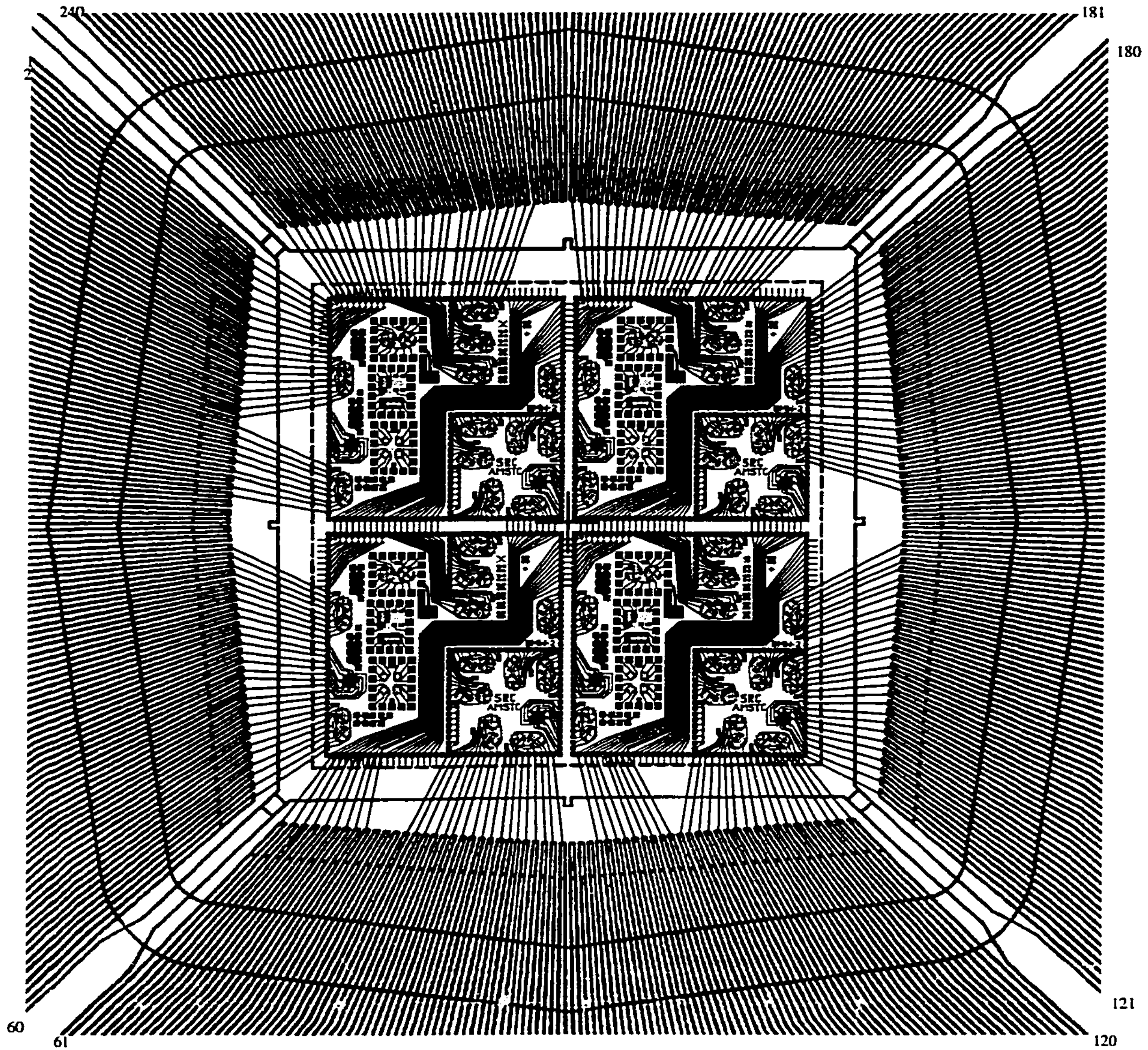

Figure 6.10 - Wiring Diagram for BMW-2 Chip in 240 Pin QFP

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were attached to the lead frame, wire bonded, and encapsulated, the post packaging room temperature resistances of the sensors were again recorded. An interface board with package socket was designed and constructed for this purpose. Using the measured resistance changes and Eqs. (4.4, 4.5), the stresses at the rosette sites on the die surface have been calculated. The test chips were from the BMW2.2 wafer lot, and the average experimentally measured piezoresistive coefficients were tabulated in Table 4.3.

A total of 103 BMW-2 test chips were encapsulated in this study. C-SAM (C-Mode Scanning Acoustic Microscopy) investigations were performed to detect delaminations at the interface between the encapsulant and die surface. Slight delaminations were found in six packages, and high degree of encapsulant voiding was found in two samples. The unusual stress readings related to packages with delaminations or encapsulant voids were removed when averaging the stress values for all of the samples at the same rosette site. The experimental stress data are presented in Figure 6.11. When compared to the previous stress measurements using AAA2 test chips, the two out-of-plane stress components σ'_{13} and σ'_{23} were extracted as well as in-plane shear stress σ'_{12} and normal stress difference $\sigma'_{11}-\sigma'_{22}$. Table 6.2 shows some significant measurement results with standard deviations. The measurement variations were noticeably smaller than those presented earlier in section 5.3.

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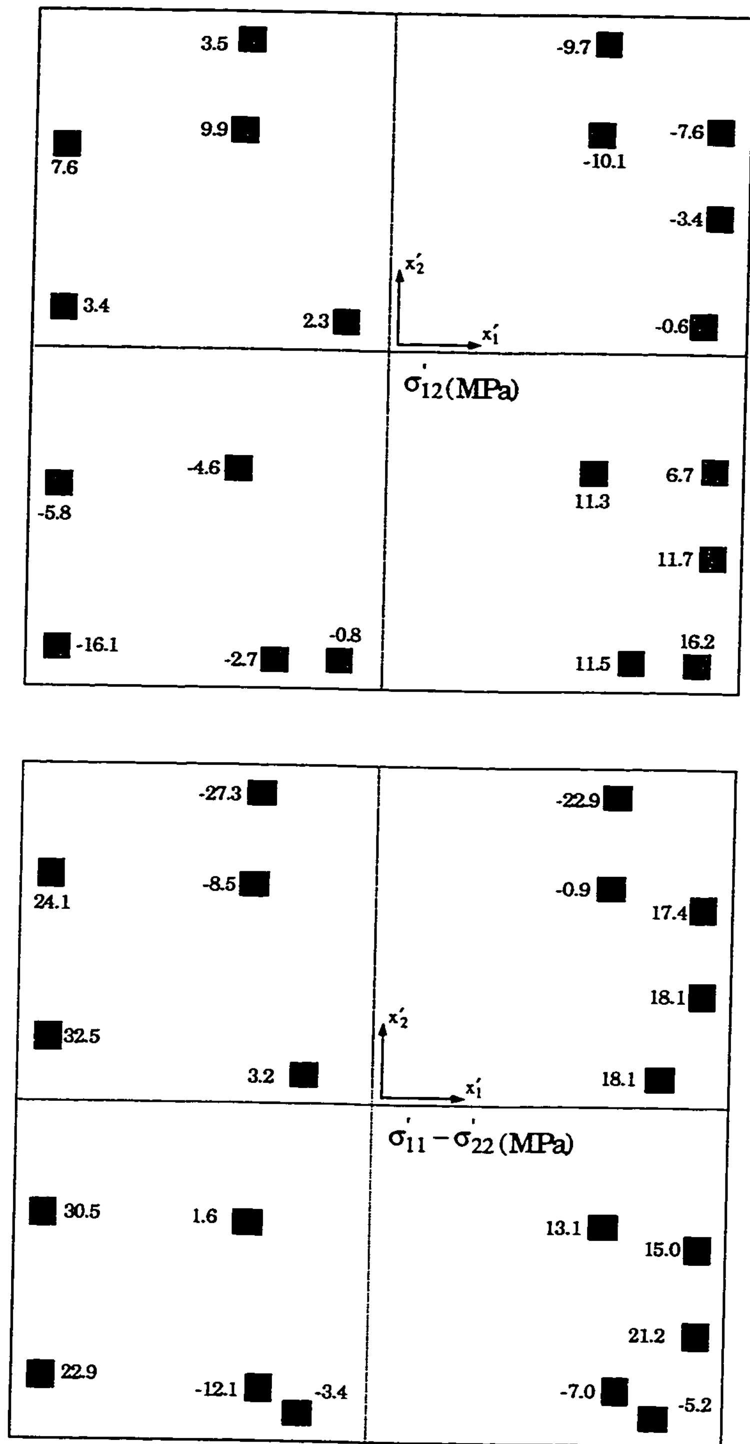

Figure 6.11 - Die Stresses After Encapsulation
(BMW-2 Chip, 240 Pin QFP)

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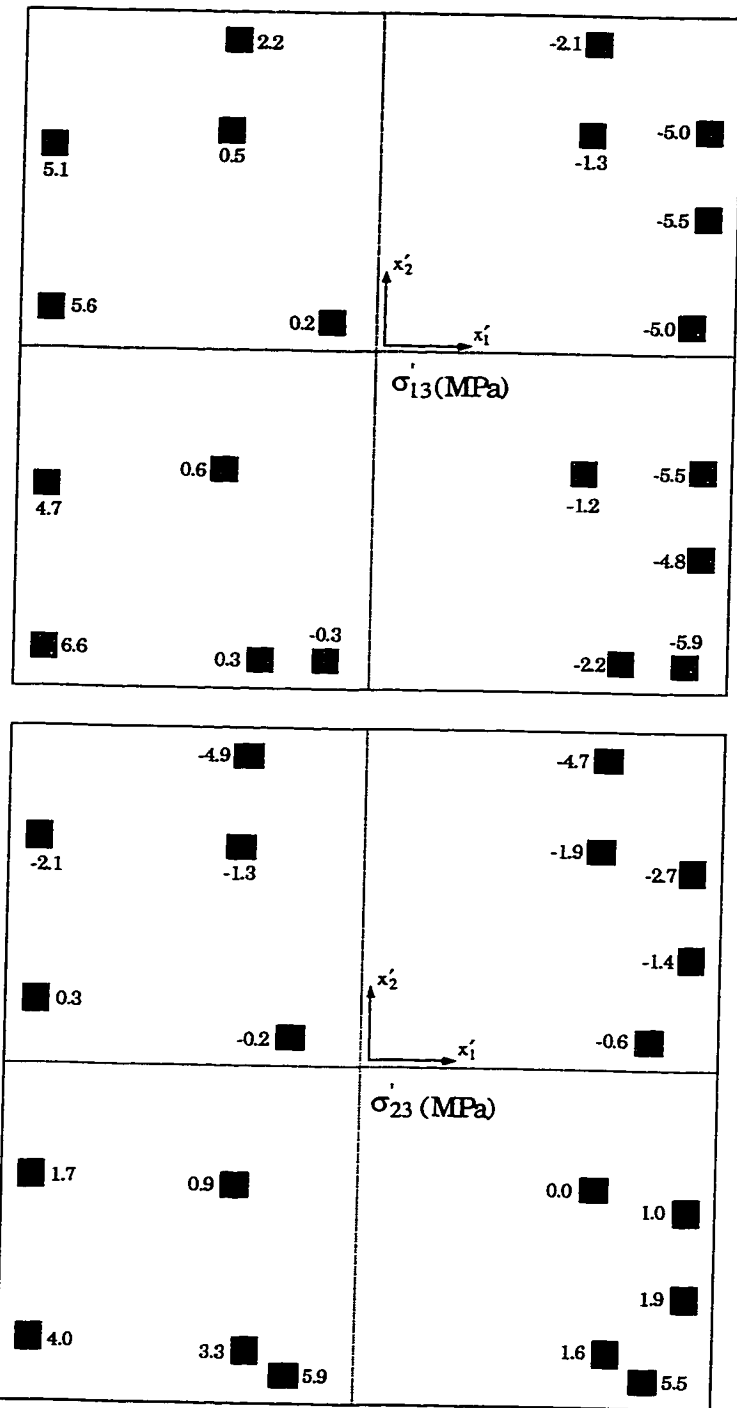

Figure 6.11 - Die Stresses After Encapsulation (Continued)
(BMW-2 Chip, 240 Pin QFP)

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Stress (MPa) (Site)	$\lvert\sigma'_{11}-\sigma'_{22}\rvert$ (Site #1)	$\lvert\sigma'_{11}-\sigma'_{22}\rvert$ (Site #2)	$\lvert\sigma'_{11}-\sigma'_{22}\rvert$ (Site #16)	$\lvert\sigma'_{12}\rvert$ (Site #4)	$\lvert\sigma'_{12}\rvert$ (Site #10)	$\lvert\sigma'_{12}\rvert$ (Site #11)
Average Stress (Std. Dev.)	24.1 (8.0)	32.5 (15.8)	22.9 (8.3)	16.1 (4.3)	16.2 (4.5)	11.7 (3.9)

Table 6.2 - Average Measured Stresses at Selected Locations with Standard Deviations (BMW-2 Test Chip, 240 Pin QFP)

The experimental results were also evaluated through correlation with the predictions of nonlinear three-dimensional finite element simulations of the package process. In the FEM models, all materials were modeled as being isotropic and linear elastic, except for the silicon die which was modeled with anisotropic material properties [134]. Temperature dependent material properties were used for the epoxy mold compound, and the values are listed in Table 6.3. Large deformations (kinematic nonlinearities) were utilized, and viscoelastic behavior of the molding compound was neglected to simplify the analysis and due to a lack of material characterization data. The die was assumed to be stress free at the glass transition temperature of the filled epoxy encapsulant, and cooling from the glass transition temperature to room temperature was simulated.

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Materials	E (GPa)	α (ppm/°C)	ν	T_g (°C)
Die attach	0.4	70	0.3	150
Lead Frame	132.4	17	0.34	
Mold Compound (-20°C)	19.8	14	0.22	155
Mold Compound (25°C)	19.3	14	0.24	
Mold Compound (60°C)	18.8	14	0.25	
Mold Compound (85°C)	17.7	14	0.26	
Mold Compound (100°C)	16.7	14	0.26	
Mold Compound (125°C)	13.9	14	0.27	
Mold Compound (155°C)	4.4	58	0.3	

Table 6.3 - Material Properties for the 240 Pin QFP (BMW-2 Study)

The dimensions of the package used in the FEM modeling are shown in Figure 6.12, and the finite element mesh (quarter model) is presented in Figure 6.13. The lead frame was simplified as a single copper pad. A copper heat slug was also present underneath the silicon die. The thicknesses of the die, die attachment material, lead frame, and heat slug were measured using a microscope. They were found to be 0.52 mm, 0.04 mm, 0.16 mm, and 0.55 mm, respectively.

Figures 6.14 - 6.17 illustrate the temperature compensated experimental data and finite element predictions for the die surface distributions of the in-plane shear stress (σ'_{12}), in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$), and out-of-plane shear stresses σ'_{13}, and σ'_{23}. In these plots, the color contours are the room temperature stress distribution predicted by the finite element models. Each of the small squares in these diagrams locates a sensor rosette site and indicates its size. The color of a given square represents the average room temperature experimental value of the stress at the rosette site, when considering the results for all the specimens used for each mold compound (the square is colored to the same

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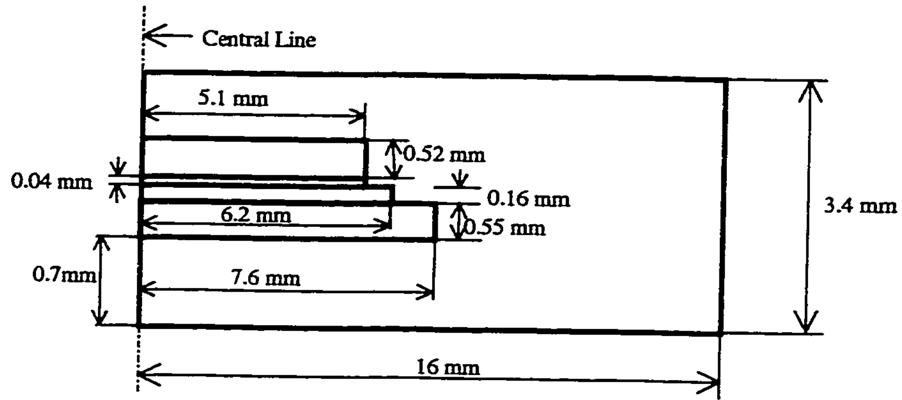

Figure 6.12 - Cross-Sectional Dimensions for the 240 Pin QFP

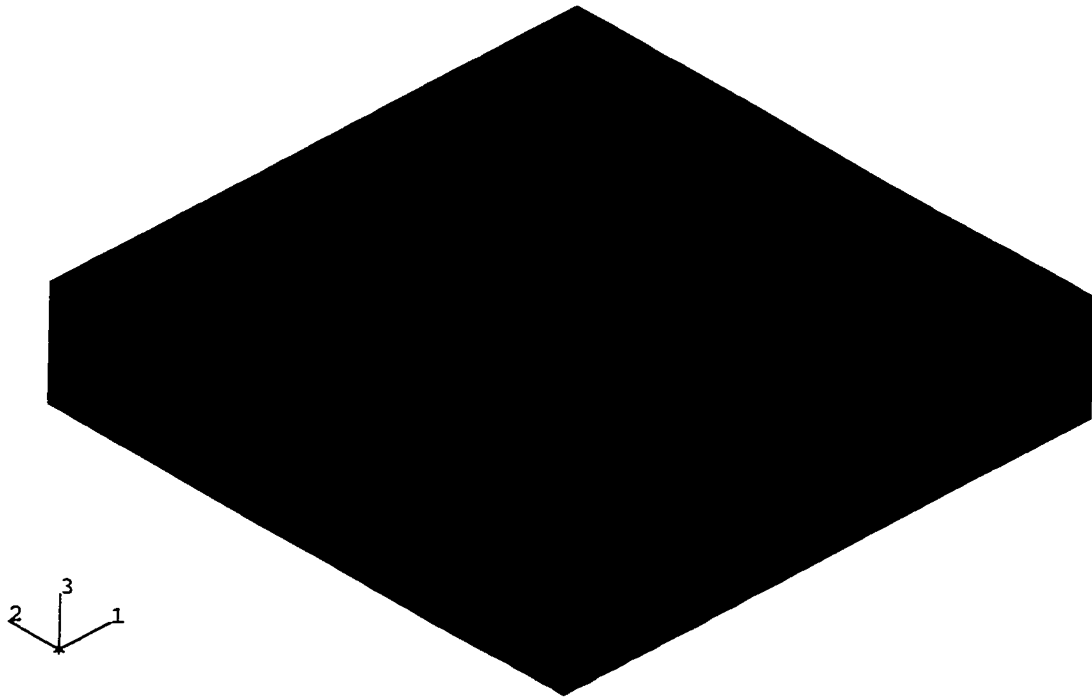

Figure 6.13 - FEM Mesh for the 240 Pin QFP
(One Quarter Model Near the Die)

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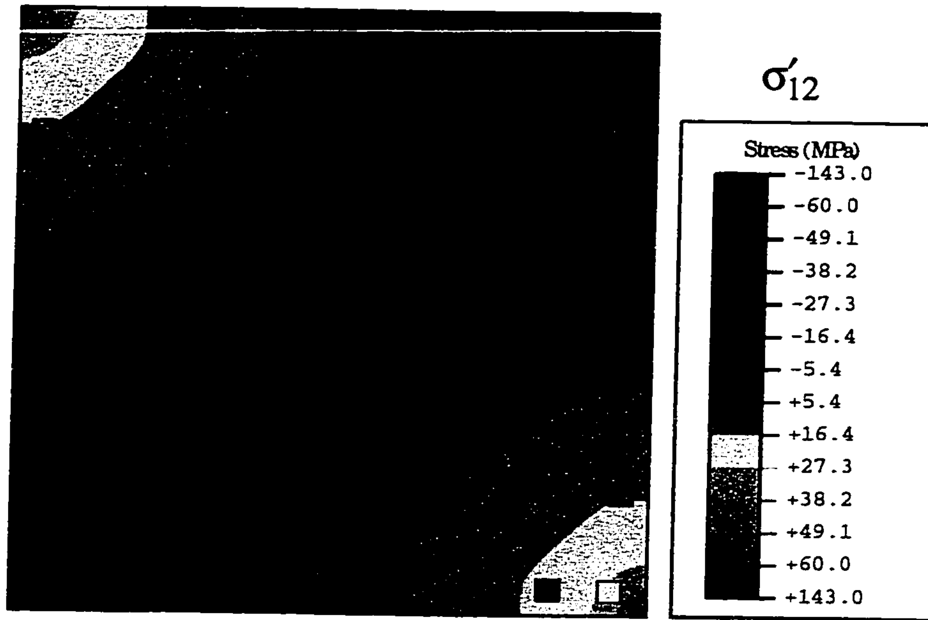

Figure 6.14 - In-Plane Shear Stress Distribution
Finite Element Contours and Experimental Data
(240 Pin QFP, BMW-2 Chip)

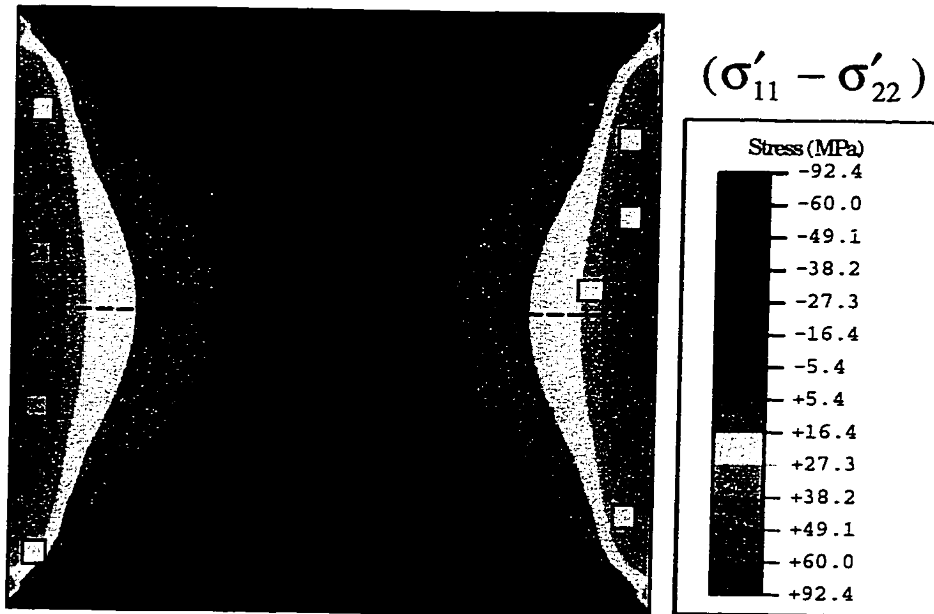

Figure 6.15 - In-Plane Normal Stress Difference Distribution
Finite Element Contours and Experimental Data
(240 Pin QFP, BMW-2 Chip)

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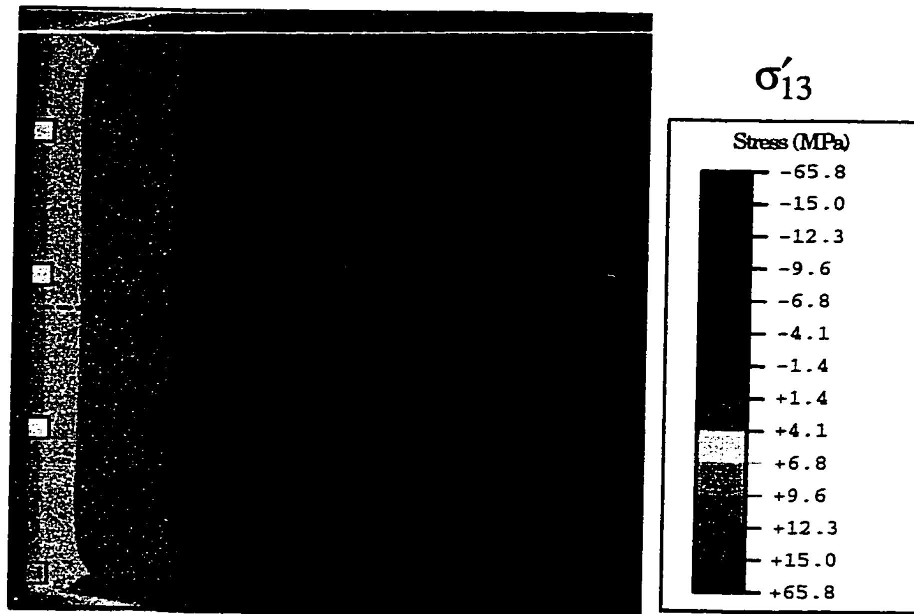

Figure 6.16 - Out-of-Plane Shear Stress σ'_{13} Distribution
Finite Element Contours and Experimental Data
(240 Pin QFP, BMW-2 Chip)

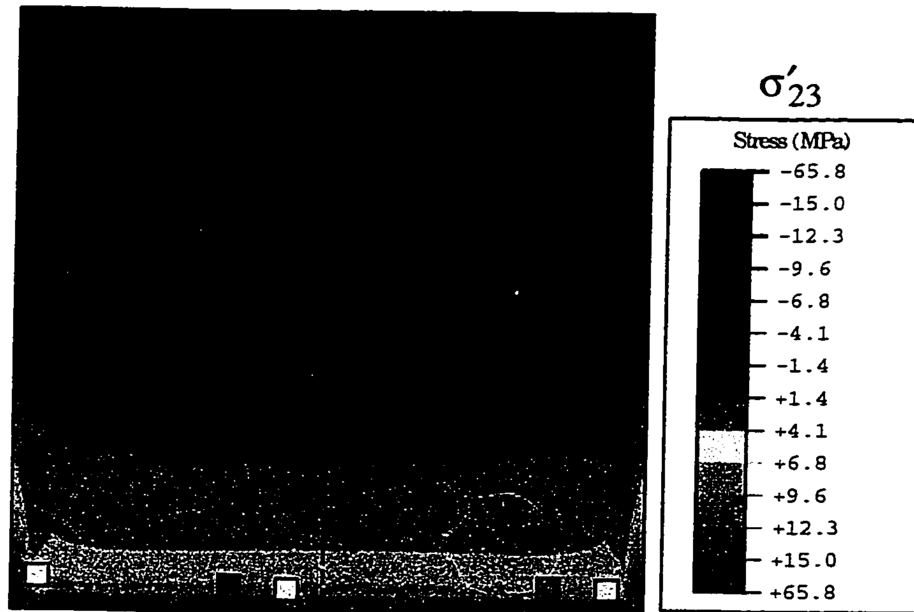

Figure 6.17 - Out-of-Plane Shear Stress σ'_{23} Distribution
Finite Element Contours and Experimental Data
(240 Pin QFP, BMW-2 Chip)

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scale/legend of the finite element contours). It can be see that the finite element predictions are in reasonable agreements with the experimental results. The measured stresses show the same trends and numerical signs as the distributions predicted by finite element analysis. The correlation of the experimental and numerical shear stress values is good. However, the finite element model over predicts the observed normal stress difference data due to the fact that viscoelastic relaxation of the filled epoxy encapsulant was neglected.

6.3 Stress Measurements in Delaminated Packages - (111) Silicon BMW-1 Test Chips

A total of ten BMW-1 test chips were packaged in the same 240 pin QFP packages as used above. In this case, the utilized test chip was a 2 x 2 array of the die schematic shown in Figure 4.6 with planar dimensions of 400 x 400 mils. The sensors at eighteen rosette sites were monitored (see Figure 6.18).

Before packaging, the initial room temperature resistances of all the sensors on the test die were recorded using an automated probe station. The characterized test chips were then bonded to the lead frame strips and encapsulated. Finally, the post packaging room temperature resistances of the sensors were recorded. Using the measured resistance changes and Eqs. (4.4, 4.5), the stresses at the rosette sites on the die surface have been calculated. The average experimentally measured piezoresistive coefficients for the utilized BMW-1 test chips are tabulated in Table 4.1.

As was done with (100) AAA2 test chip and (111) BMW-2 test chip samples, the data for each rosette site and each stress component were averaged. While the AAA2 and

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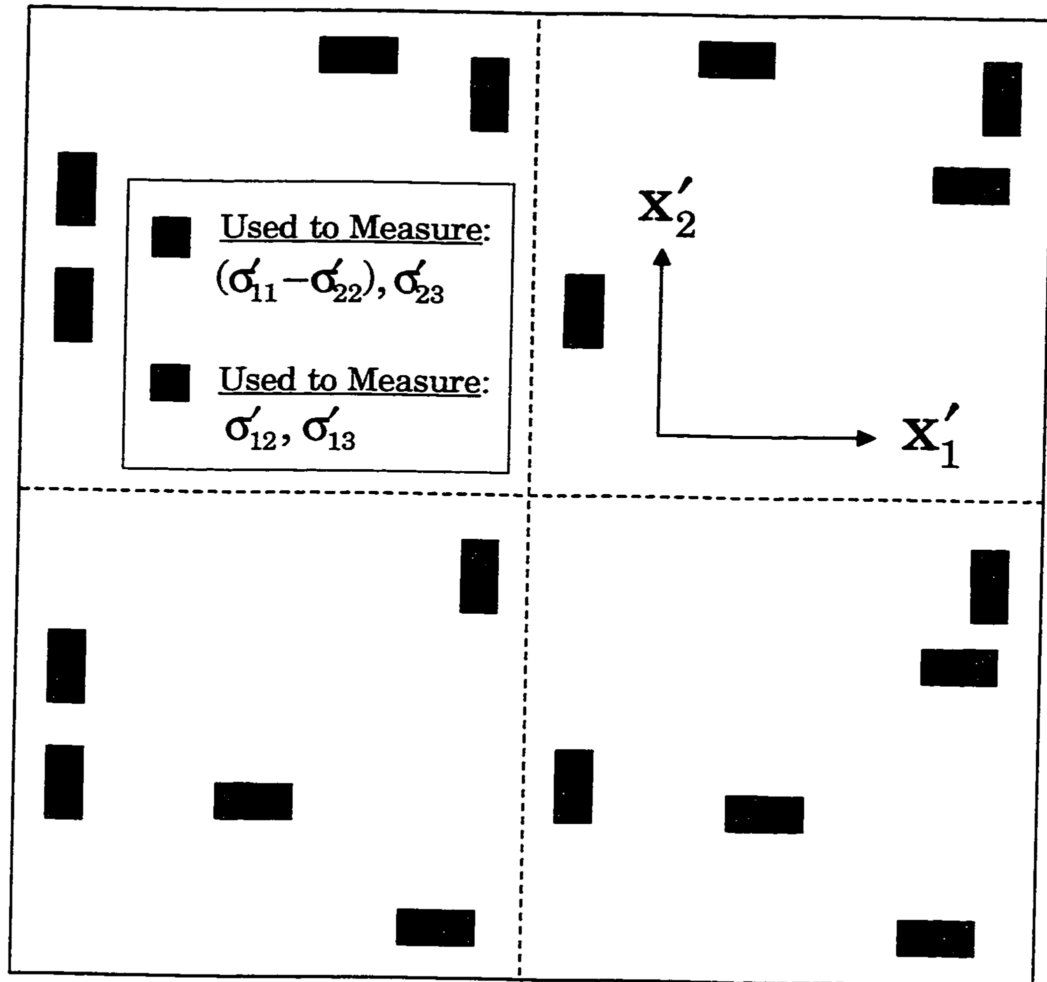

Figure 6.18 - BMW-1 Sensor Rosette Locations
(400 x 400 mil Test Chip, 240 Pin QFP)

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BMW-2 test chip data were fairly tightly grouped for a given stress component and rosette location, the results extracted from the BMW-1 test chip data showed wide variation. The experimental results did not seem to follow expected trends, and large standard deviations were observed. When compared to the prediction of finite element simulations of the packaging process, some of the average experimental stress values had the "wrong" algebraic sign. Also, many of the sensors near the edge of the die had experienced large resistance changes, and several sensors appeared to have become open-or-short circuited.

Due to inconsistencies in the data, it was assumed that delaminations had probably occurred between the silicon die and the molding compound, and that many of the sensors had been damaged. The packages were sent for C-SAM evaluation, and delaminations between the top surface of the die and the mold compound were found in all of the packages. The delaminated region of the packages ranged from 18% to 100% of the total area. Photos of the C-SAM images are shown in Figure 6.19 (red indicates delamination) along with overlays showing the locations of the sensor rosettes. Also, the fractional percentages of the die surfaces that were delaminated are listed in Table 6.4.

Sample	% Delaminated Area
1	18%
2	24%
3	58%
4	25%
5	100%
6	43%
7	33%
8	100%
9	100%
10	23%

Table 6.4 - Delaminated Regions in the Encapsulated BMW-1 Test Chips

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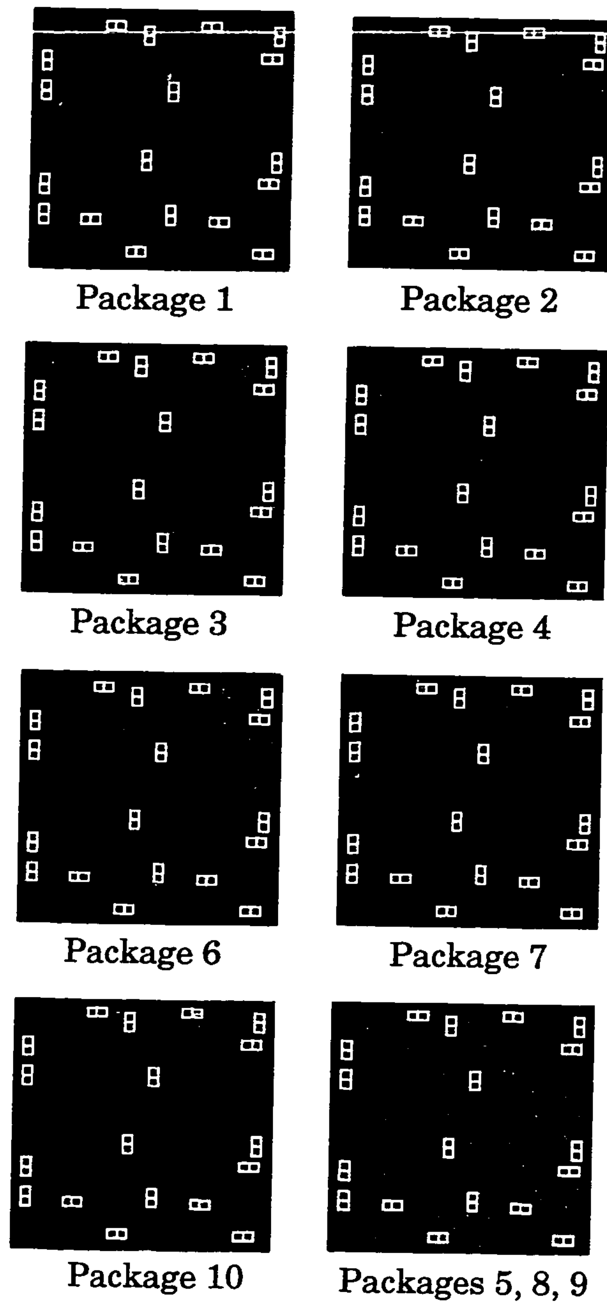

Figure 6.19 - C-SAM Images of the Encapsulated BMW-1 Test Chips (240 Pin QFP)

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One probable cause of these delaminations was the fact that the BMW-1 test chips used in this study were not passivated. Although we typically use polyimide or silicon nitride passivations, non-passivated die were chosen in this study to examine the effects of the passivation on the total stresses accumulated in a plastic packaged die. Since mold compounds are optimized for adhesion to standard die passivation materials, it is likely that poor bonding of the mold compound to the non-passivated die surface resulted. As discussed above, no delaminations were found in the packages fabricated using the (100) AAA2 test chips. These die were coated with a 2 μm thick polyimide passivation layer. In the BMW-2 experiments discussed above, a 2 μm thick silicon nitride passivation layer was used on the test chips, and only limited delaminations were observed.

It can be seen from the photos in Figure 6.19 that three of the specimens were totally delaminated (packages 5, 8, 9). Also, all of the die became debonded from the encapsulant at their corners, where high shear stresses are known to occur. Most of the die were also delaminated along their entire perimeter. The delamination areas were highly varied in size and shape, and were not symmetrical. The presence of interfacial cracks and debonds will greatly shift the local stress, strain, and deformation fields near the die/encapsulant interface. The BMW-1 piezoresistive sensor rosettes are located right at this interface, and the delaminations varied from package to package. Therefore, it is difficult or impossible to make conclusions using the average stress sensor data from particular rosette sites. As was noted above, sensors in delaminated regions were often damaged (due to the interfacial crack growth and lack of passivation) and open- and short-circuited rosettes were often found.

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For each sample, rosette sites on the embedded test chip that were in non-delaminated regions were identified with the aid of the C-SAM images. The stresses calculated at the non-delaminated rosette sites were then averaged over all of the packages. Figures 6.20-6.21 illustrate temperature compensated experimental measurements and finite element predictions for the die surface distributions of the in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$) and the in-plane shear stress σ'_{12}. In these plots, the color contours are the room temperature stress distributions predicted by the finite element model for a totally non-delaminated package. The finite element calculations were from the same model as discussed in the previous section for the BMW-2 test chip experiments. Each of the small squares in these diagrams locates a sensor rosette site. The color of a given square represents the average room temperature experimental value of the stress at the rosette site, but only data from non-delaminated sites were included in the averaging process. As before, the squares are colored to the same scale/legend of the finite element contours. If all of the packages were delaminated at a particular rosette site (e.g. at rosette sites near the corners of the chips), an "X" was placed through the square.

In Figure 6.20, the in-plane shear stress data are all small in value. Delamination had occurred at all of the rosette sites that would have been expected to have high in-plane shear stress magnitudes (near the die corners). Some of the sites also show average data with algebraic signs opposite to those predicted by the finite element calculations. It is clear that delaminations will greatly perturb the in-plane shear stress distribution on the top surface of the die. The results for the in-plane normal stress difference in Figure 6.21 show many similarities to the data from non-delaminated packages obtained with AAA2 or

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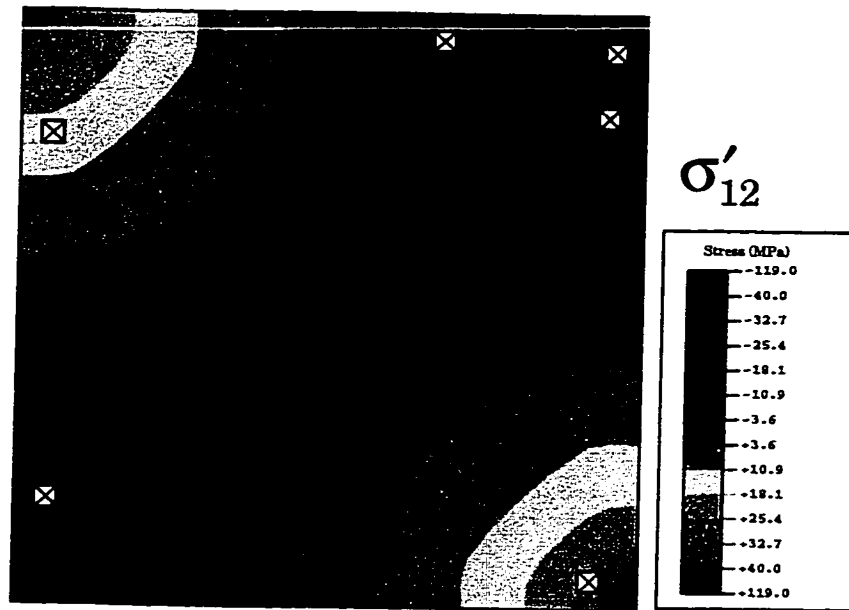

Figure 6.20 - In-Plane Shear Stress Distribution, Finite Element Contours and Experimental Data (BMW-1, 240 Pin QFP)

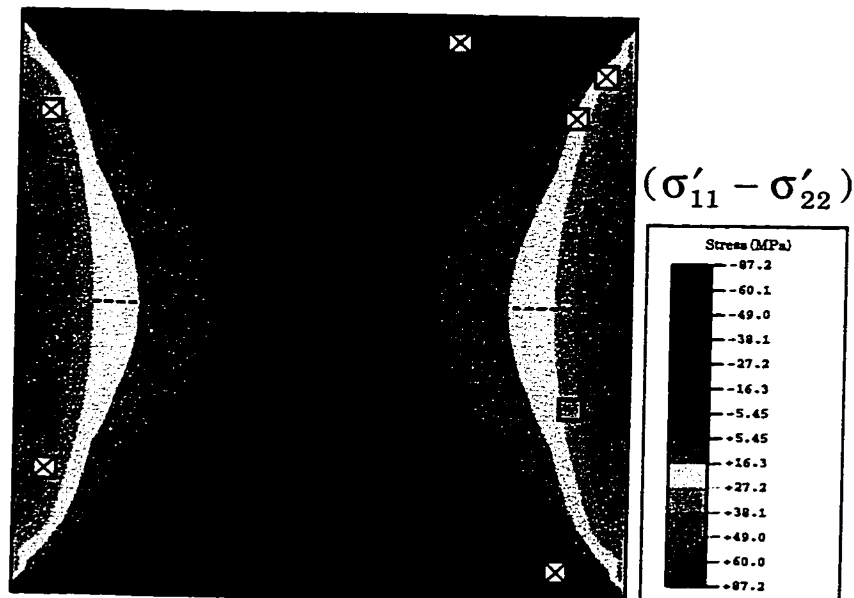

Figure 6.21 - In-Plane Normal Stress Difference Distribution, Finite Element Contours and Experimental Data (BMW-1, 240 Pin QFP)

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BMW-2 test chips shown in Figure 6.8 and Figure 6.15. The finite element predictions show the same trends as the experimental data. However, the simulations typically over predict the observed normal stress difference data due to the facts that the viscoelastic relaxation of the filled epoxy encapsulant was neglected. In these delaminated packages, this discrepancy is further exacerbated since the actual die stresses are reduced due to the decreased efficiency of loading transmitted by the encapsulant to the die. These conclusions are consistent with those made by Miura, et al. [36]

A new feature of (111) silicon test chips is the ability to measure the out-of-plane (interfacial) shear stresses σ'_{13} and σ'_{23}. In non-delaminated die, these stresses are relatively small, except very near the die edges (Figure 6.16 and Figure 6.17). In measurements in chip on board packages [82, 117], the magnitudes of these stresses were also typically in the range of 0-6 MPa. However, in the delaminated QFP's studied here, the magnitudes of these stresses became very high (up to 50 MPa). This was especially true at non-delaminated rosette sites that were very near the edge of the delamination region. These observations are demonstrated in Figure 6.22, where the measured magnitudes of the total out-of-plane shear stress are displayed for one of the delaminated samples.

6.4 Summary

In this study, special (100) and (111) silicon test chips containing arrays of optimized piezoresistive stress sensor rosettes have been used to characterize die surface stresses in 240 pin QFP packages. The sensors on the (100) test chips were able to

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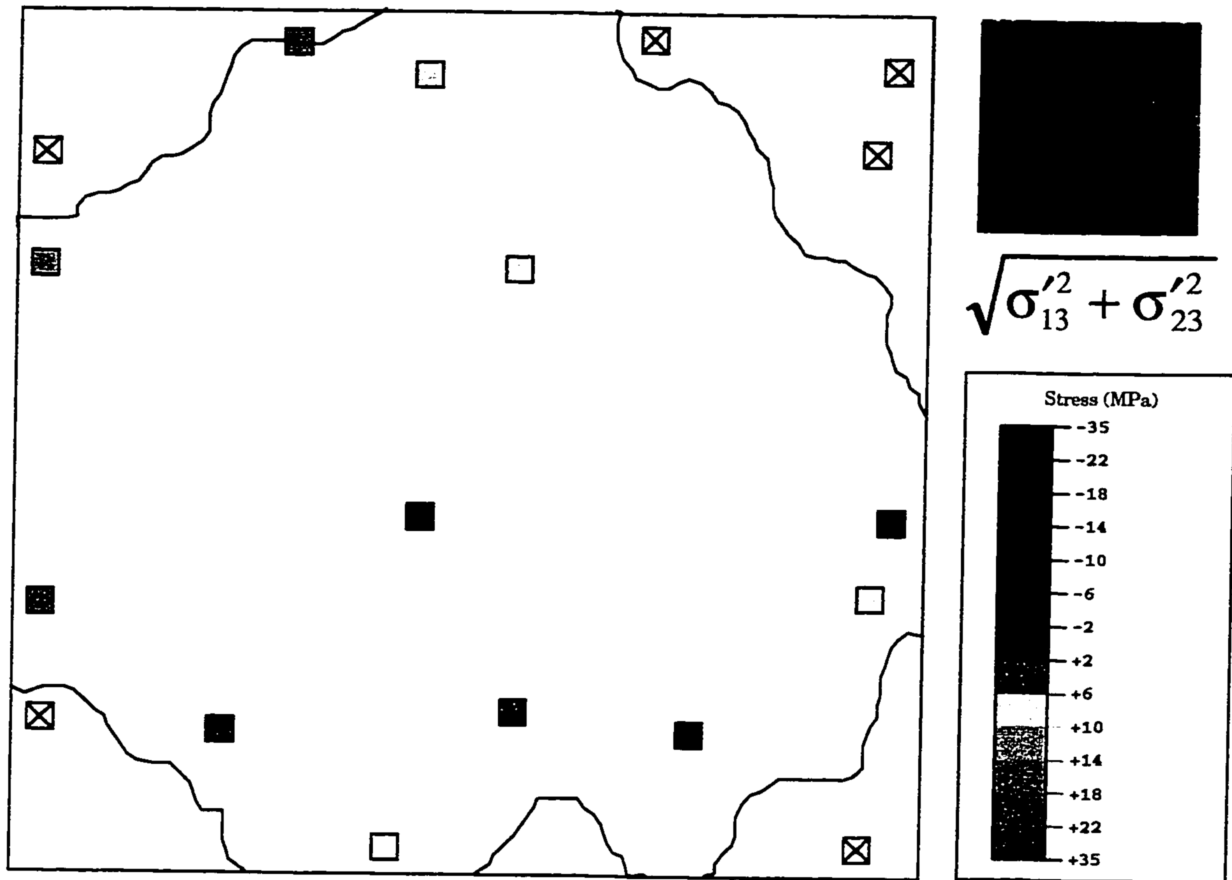

Figure 6.22 - Total Out-of-Plane Shear Stress Data for a Typical Delaminated Die (Package #1, BMW-1, 240 Pin QFP)

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accurately measure two in-plane stress components in a temperature compensated manner, while the rosettes on the (111) test chips were uniquely capable of evaluating all the 6 stress components, four in a temperature compensated manner. Calibrated and characterized (100) and (111) test chips were encapsulated in 240 pin quad flat packs (QFP's). The post packaging room temperature resistances of the sensors were then recorded. The stresses on the die surface were calculated using the measured resistance changes and the appropriate theoretical equations. For comparison purpose, three-dimensional nonlinear finite element simulations of the plastic encapsulated packages were also performed. The presence of delaminations between the die surface and the encapsulant was explored using C-Mode Scanning Acousic Microscopy (C-SAM).

In the (100) AAA2 test chip and (111) BMW-2 test chip experiments, few delaminations occurred. The correlation of the experimental and numerical in-plane shear stress values was excellent. However, the finite element model over predicted the observed normal stress difference data due to the fact that that viscoelastic relaxation of the filled epoxy encapsulant was neglected. These conclusions are consistent with those obtained in other studies for different encapsulated packages. Delaminations occurred between the silicon die and the molding compound for all of the QFP samples prepared with (111) BMW-1 test chips. Many of sensors in the delaminated regions were damaged. Measured in-plane stresses in non-delaminated regions showed similar magnitudes but were perturbed from values expected in packages without delamination boundaries. The out-of-plane shear stresses in delaminated packages were found to be much higher than in non-

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delaminated packages, and can serve as a method for detecting and characterizing delaminations.

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CHAPTER 7

IN-SITU STRESS STATE MEASUREMENTS DURING CHIP-ON-BOARD ASSEMBLY

7.1 Introduction

Chip-on-Board (COB) technologies, where semiconductor die are attached directly to a second level substrate (e.g. ceramic or organic circuit board), have become popular for MCM applications requiring reliable packaging with reasonable costs. The first level chip package is eliminated altogether and processing is often simplified. Multiple IC chips and passive components are typically incorporated together on a common substrate to reduce board I/O counts. Relative to surface mount and through-hole designs, the more efficient use of board area in COB packaging technology leads to shorter interconnections, faster speeds, and reduced package size.

In wire bonded COB packaging (chip-and-wire), the chip level interconnect is done by wire bonding. The chip is attached to the substrate with a die attachment adhesive (e.g. silver-filled epoxy), and the outer leads are then bonded. Finally, the die is encapsulated using a "glob-top" liquid encapsulant (see Figure 7.1).

Stress test chips based on piezoresistive sensors have been used by several investigators to examine the die stresses caused in wire bonded COB packaging processes. Sweet and co-workers [96-98] have used the (100) silicon Sandia ATC-04 test chip to

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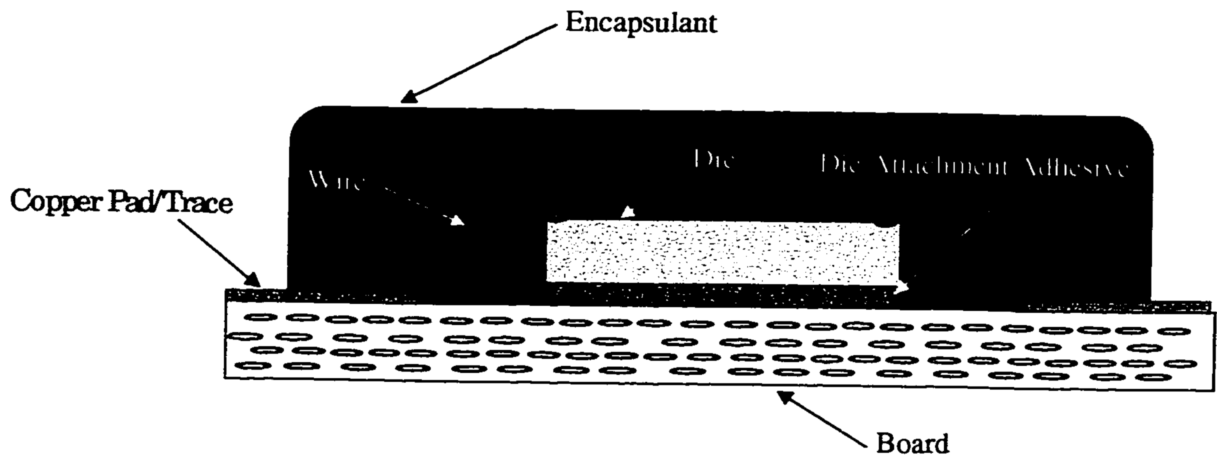

Figure 7.1 - Wire Bonded COB

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investigate liquid encapsulation of integrated circuit die mounted directly on ceramic substrates. Room temperature stresses were evaluated after both the die attachment and encapsulation processes. In their experiments, the substrate was a 40 pin ceramic DIP, and two liquid encapsulants were studied. Suhling, et al. [81, 116] have used the (111) silicon BMW-1 test chip to make measurements of the complete state of stress in encapsulated die which were attached to FR-4 substrates. In addition to the in-plane stress components measured in the Sandia studies, the out-of-plane (interfacial) shear stresses at the die to encapsulant interface were recorded. Again, the stress measurements due to both the die attachment and die encapsulation processes were made at room temperature. In addition, a demonstration of the variation of the die surface stresses with package temperature was also made. Results were correlated with the predictions of finite element simulations. No previous study on COB die stresses has examined the in-situ stress variation occurring during the encapsulant cure process.

In this work, (111) silicon test chips have been used to characterize the variation of die stress throughout the COB packaging process. The initial sensor resistances were recorded when the test die were in wafer form. The rosettes were later characterized after die attachment, and throughout the cure cycle of the liquid encapsulant. Using the measured data and appropriate theoretical equations, the stresses at sites on the die surface have been calculated. Also, preliminary three-dimensional nonlinear finite element simulations of the chip-on-board packages were performed, and the stress predictions were correlated with the experimental test chip data.

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7.2 Chip-on-Board Packaging Studies

The BMW-2 stress test chips used in this study had planar dimensions of 400 x 400 mils (a 2 x 2 array of the die schematic shown in Figure 4.8). They were first directly bonded to FR-4 printed circuit board (PCB) substrates using a silver-filled epoxy die attachment adhesive (Ablestik Ablebond 84-1LMI). Gold wires were then used to provide the interconnections from the die bond pads to the metal traces on the PCB's. Finally, the die were encapsulated using a "glob-top" epoxy coating. In this investigation, two different liquid encapsulants manufactured by Dexter Electronic Materials Division were considered. The first was Hysol FP4450, with a room temperature coefficient of thermal expansion (CTE) of $\alpha = 22 \times 10^{-6}$ 1/°C. The second material was Hysol FP4650, which is based on the same chemistry, but features an improved resistance to moisture adsorption and a lower room temperature CTE of $\alpha = 15 \times 10^{-6}$ 1/°C.

A total of 30 specimens were prepared. Although there are 20 accessible rosette sites on the 400 x 400 mil BMW-2 die, only eight were utilized in this study due to line width and routing limitations on the PCB. The copper traces on the PCB were routed to the edge of the board, and a standard edge connector was used to provide electrical connection of the samples to a data acquisition system. Figure 7.2 shows a typical COB specimen from this study, and Figure 7.3 shows the selected rosette sites for stress measurement.

Before packaging, the initial room temperature resistances of all of the sensors were recorded when the chips were in wafer form using an automated probe station. The characterized test die were then diced from the wafers and bonded to the PCB's. After die attachment and wire bonding, the sensor resistances were again measured. Finally, the

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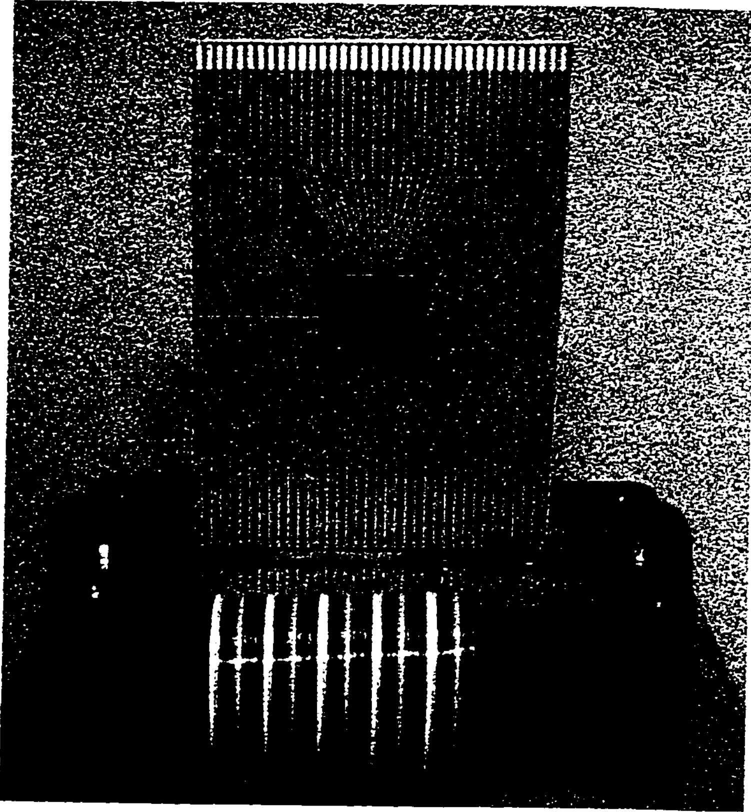

Figure 7.2 - Chip-On-Board Specimen with Encapsulated Test Chip

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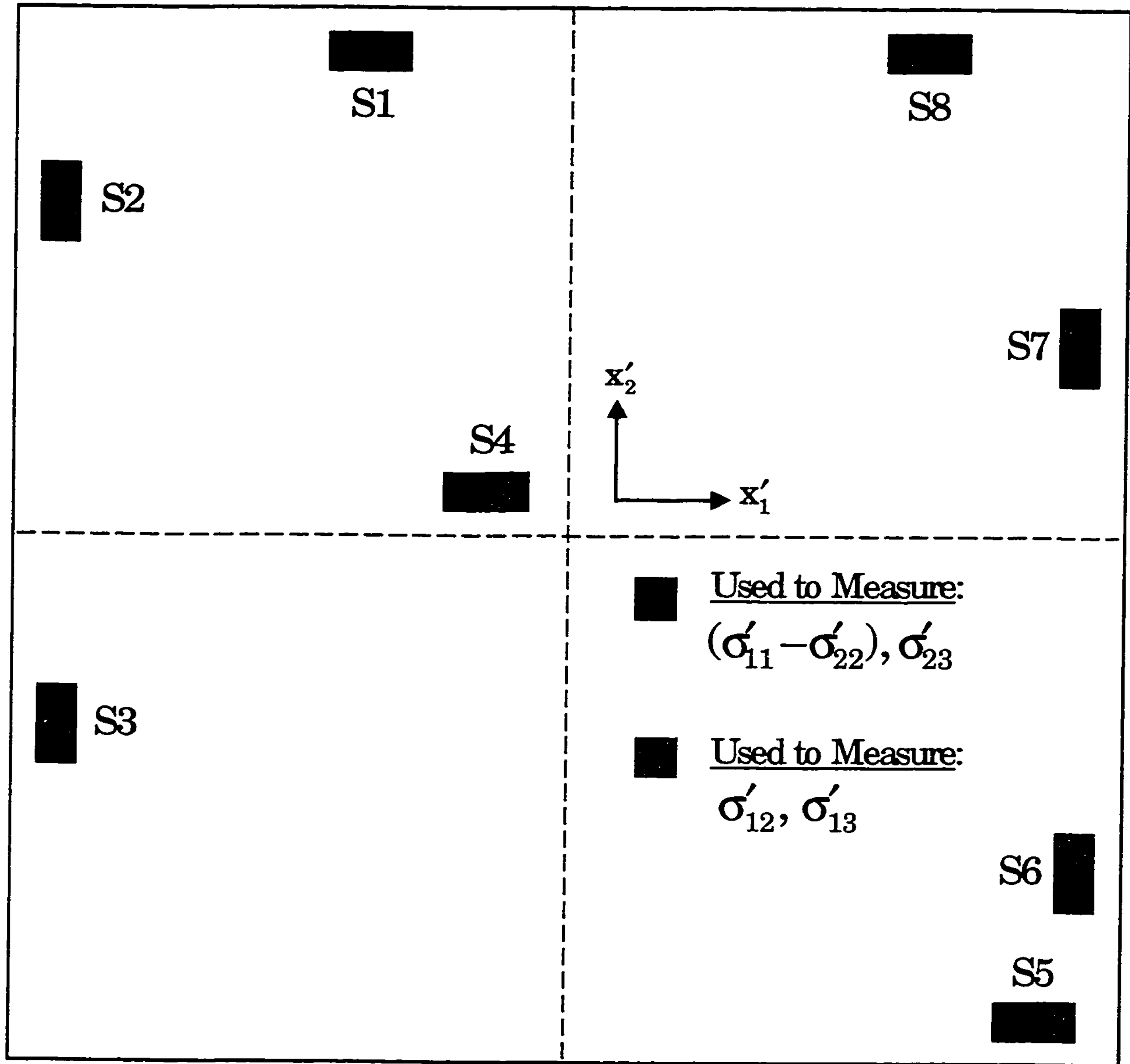

Figure 7.3 - Sensor Rosette Locations (400 x 400 mil Test Chip, COB)

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liquid encapsulants were applied and the samples were cured in an oven. The substrates were warmed on a hot plate to a temperature of 80 °C while the encapsulants were dispensed. The cure cycle consisted of a two step process: 30 minutes at 125 °C and then 90 minutes at 165 °C. After removal from the cure oven, the samples were cooled to a normal room temperature environment of 23 °C. Sensor resistances were monitored during the entire encapsulant cure process, and the post packaging room temperature resistances of the sensors were recorded. Using the measured resistance changes and Eqs. (4.4, 4.5), the stresses at the rosette sites on the die surface were calculated at the various steps in the COB packaging process.

7.3 Stresses Due to Die Attachment

After the test chips were bonded to the FR-4 substrates, the die attachment adhesive was cured for 60 minutes at 150 °C per vendor instructions. The specimen assemblies were then cooled to room temperature and the gold wire bonding was performed to interconnect the perimeter bond pads on the die to the substrate traces. Sensor resistances were recorded, and the room temperature die surface stresses induced by the die attachment process were calculated using these measurements and the resistance data recorded while the die were still in wafer form.

The measured values of the in-plane shear stress σ'_{12} and the in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$) are shown in Figure 7.4. Each indicated value is the average of data taken from the 30 specimens. The magnitudes are universally small when compared to the stresses typically induced by topside encapsulation, where the sensor

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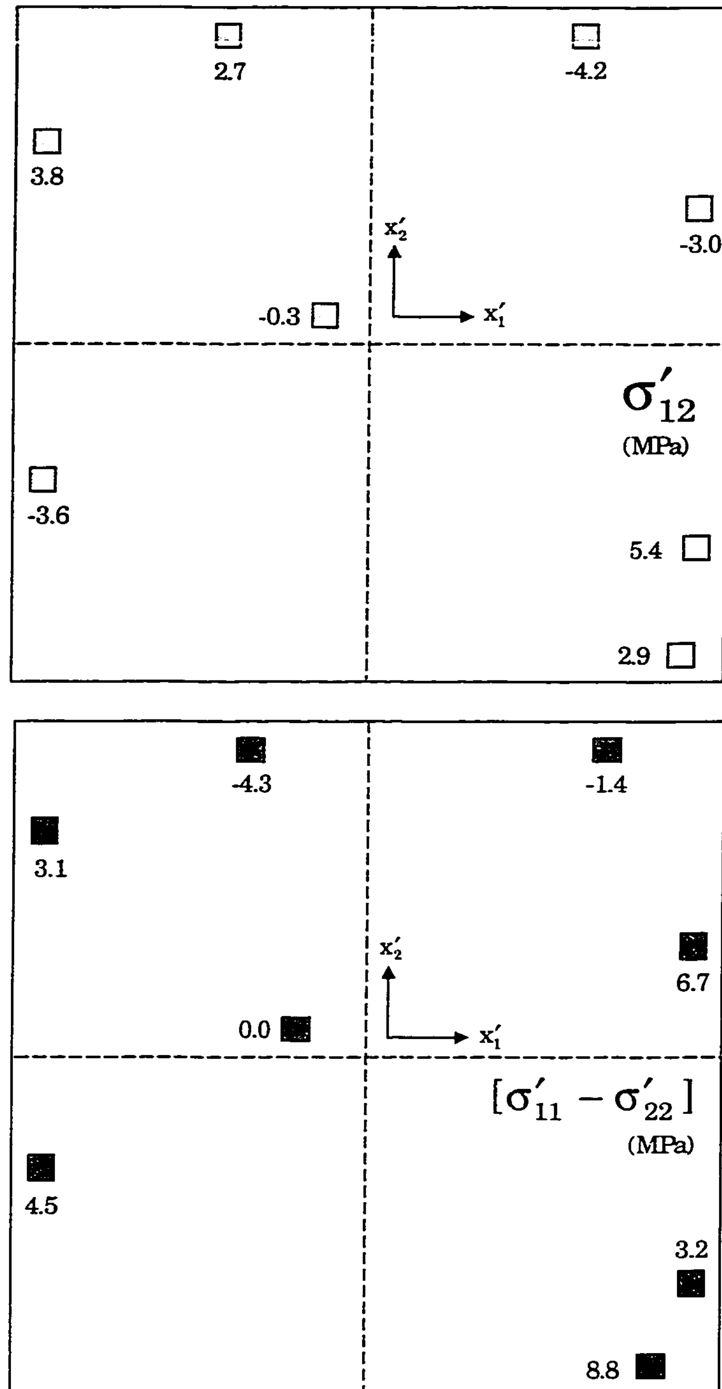

Figure 7.4 - Measured Stresses Caused by Die Attachment (COB)

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surface is contacted directly by a material of drastically different CTE. In addition, the average measured magnitudes of the out-of-plane shear stresses σ'_{13} and σ'_{23} were typically less than 1 MPa, a level that approaches the resolution limit of the experimental method. Note that these shear stresses are theoretically zero at this point in the packaging process, due to the fact that the die surface is still free of shear contractions.

The die surface stress data shown in Figure 7.4 are similar in nature to the room temperature stress distributions induced in plastic packages by total encapsulation of the die by a mold compound [23]. However, they are much less in magnitude. Figure 7.5 illustrates the idealized signs of the various die stress components in a plastic encapsulated package. The in-plane shear stress distribution on the top surface of the die in a plastic encapsulated package is negative in quadrants 1 and 3, and positive in quadrants 2 and 4 (see Figure 7.5). The shear values are zero at the center of the die, and on the horizontal and vertical symmetry lines (dotted). The magnitude of the shear stress increases as the corners are approached. The idealized normal stress difference distribution is zero along the die diagonals, and alternates positive and negative as also shown in Figure 7.5. The difference magnitudes increase as the centers of the sides are approached. It is observed that the chip on board die attachment stress data shown in Figure 7.4 follow the trends discussed above and symmetries shown in Figure 7.5 for plastic encapsulated die. This analogy was also predicted theoretically as discussed below.

The stress distributions present after die attachment are predominately a result of the differential thermal expansion between the silicon die and FR-4 substrate. When the

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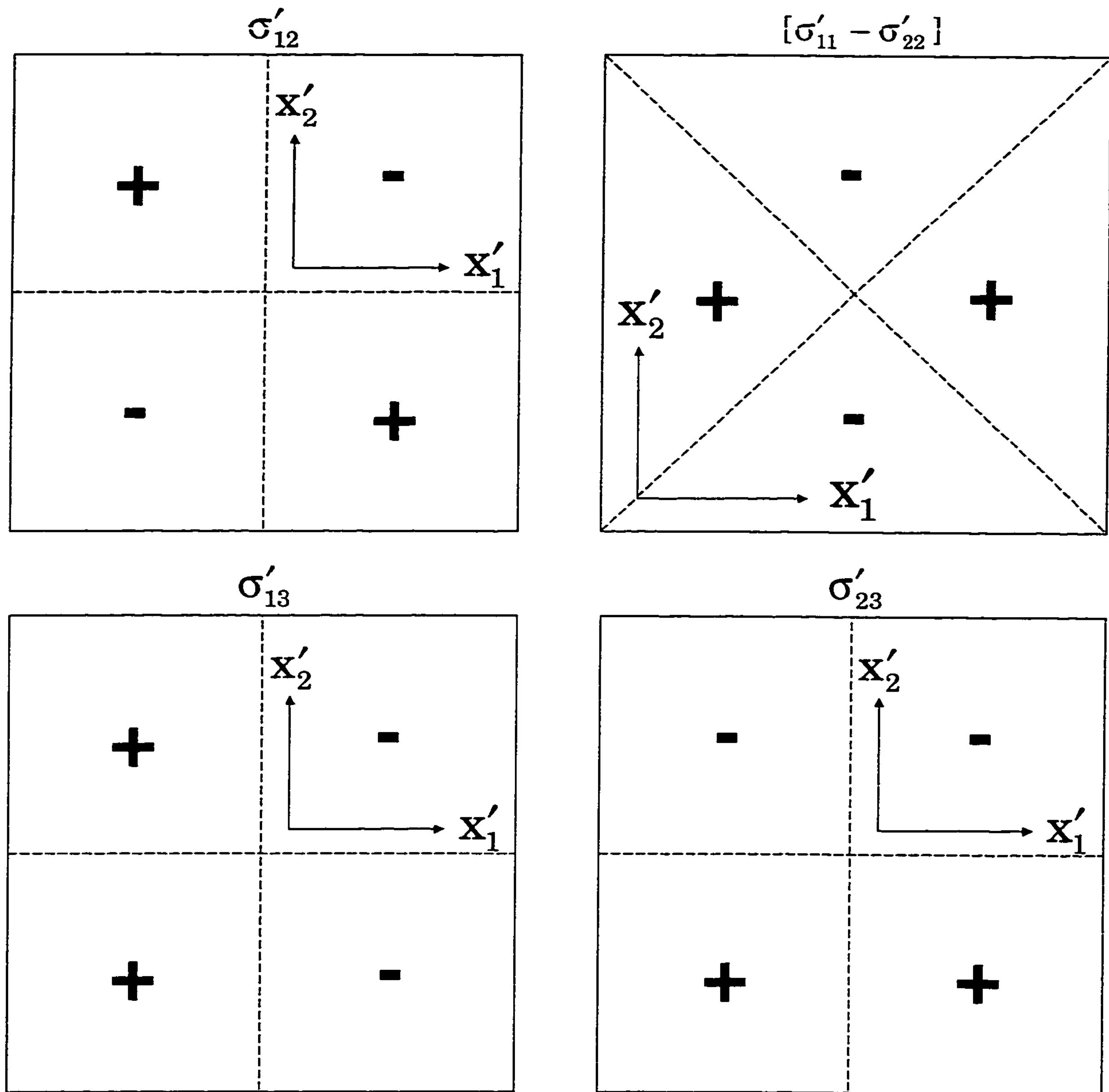

Figure 7.5 - Signs of Idealized Encapsulated Die Stress Distributions

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three-material system is initially raised to the die attach cure temperature, the adhesive is uncured so that the die and substrate are nearly stress free. When the bonded assembly is cooled down to room temperature after the adhesive is cured, thermal stresses are generated due to the differential shrinkages resulting from the differences in the coefficients of expansion of the die (α = 2.3 x 10^{-6} 1/°C), die attach (α = 55 x 10^{-6} 1/°C), and FR-4 substrate (α = 13 x 10^{-6} 1/°C). During the cooling, the substrate would like to contract much more than the silicon. If the bonded tri-material stack remains flat, it is clear that the silicon will be subjected to compression and the substrate to tension (in all in-plane directions). However, such unsymmetrical laminates will also warp/bend under temperature change, especially for thin FR-4 substrates. For the given system, the resulting bending deformations will tend to subject the topside of the die to in-plane tension and the bottom side of the PCB substrate to in-plane compression. Thus, the stresses resulting from the bending deformations are opposite in nature to those occurring due to purely in-plane membrane deformations. The realized stresses on the die surface are a combination of such counteracting membrane and bending effects, and are further effected by the anisotropic material behavior of the FR-4 laminate and silicon die.

The actual magnitudes and signs of the die surface stresses will depend in a complicated manner on the expansion coefficients, thicknesses, and elastic moduli of the FR-4, silicon, and die attachment material. For the assemblies in this work, the substrate thickness was .062 inches (1.5mm) and the die thickness was .021 inches (0.52mm). Finite element modeling and lamination theory calculations have both been used to predict that the membrane effects dominate the bending effects for this configuration. Thus, the silicon

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should be subjected to a nominal compression in all in-plane directions. This is similar to chips in plastic encapsulated packages and validates the experimental measurements discussed above. However, it is also noted that the signs of the die stresses predicted theoretically will be reversed if thinner substrates are used. We have also observed this experimentally for die that are attached to thin copper lead frames or thin FR-4 substrates.

Finite element modeling results for COB die attachment samples are now presented to show the effects of package geometry on the die surface stresses resulting from die attachment. Several thicknesses of the COB FR-4 substrate were modeled including 0.5 mm, 0.7 mm, 1.0 mm, 1.5mm, 2.5 mm, and 4.5 mm. The actual thickness was 1.5 mm. To simplify the modeling, all materials were modeled as linear elastic. Also, temperature dependent material properties for the die attachment adhesive were included. The thicknesses of the die and die attachment adhesive were 0.52 mm and 0.12 mm, respectively, in all of the models. The dimensions of the actual samples are shown in Figure 7.6, and the material properties are listed in Table 7.1. The assembly was assumed to be stress free at the glass transition temperature of the die attachment adhesive, and cooling from that point to room temperature was modeled.

The FEM simulation results for the various substrate thicknesses are presented in Figure 7.7. The predicted maximum in-plane shear stress (σ'_{12}) on the die surface becomes larger when the thickness of the board changes from 0.5 mm to 1.5 mm, and then decreases when the board thickness changes from 2.5 mm to 4.5 mm. The maximum in-plane normal stress difference on the die surface continues to increase when the board thickness becomes larger. However, an algebraic sign change in the in-plane normal stress difference is also

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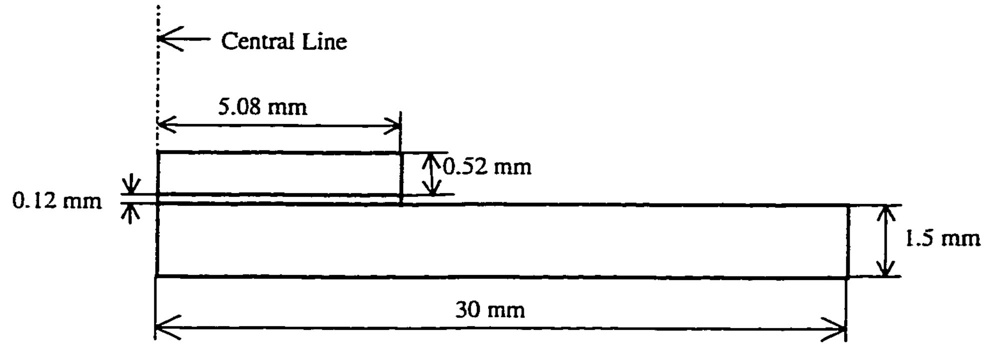

Figure 7.6 - Dimensions of COB Die Attachment Model

Materials	E (GPa)	α (ppm/°C)	ν	T_g (°C)
Die	131.0	2.6	0.28	
FR-4 Board	17.9	20	0.28	
Adhesive (-25°C)	10.1	57	0.4	150
Adhesive (0°C)	9.34	57	0.4	
Adhesive (25°C)	8.26	57	0.4	
Adhesive (50°C)	6.30	57	0.4	
Adhesive (75°C)	1.96	57	0.4	
Adhesive (100°C)	1.05	57	0.4	
Adhesive (125°C)	0.74	57	0.4	
Adhesive (150°C)	0.54	57	0.4	

Table 7.1 – Material Properties for the COB Die Attachment Models

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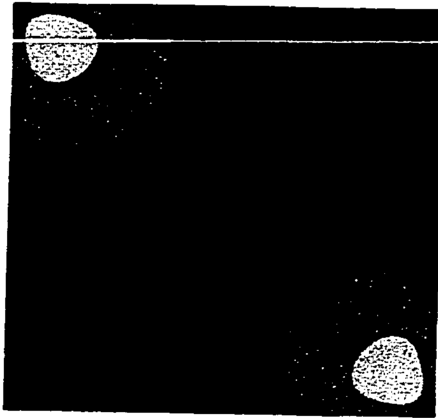
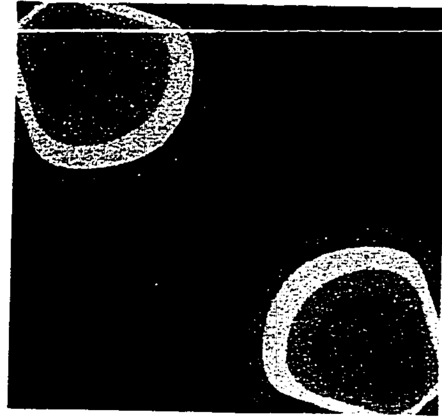
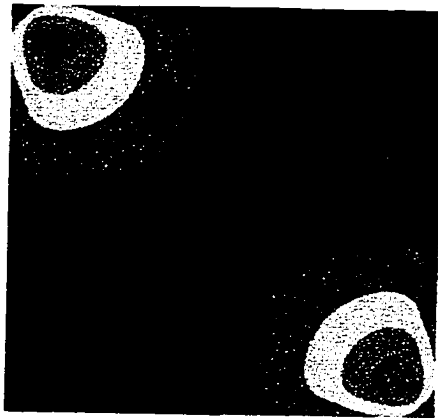


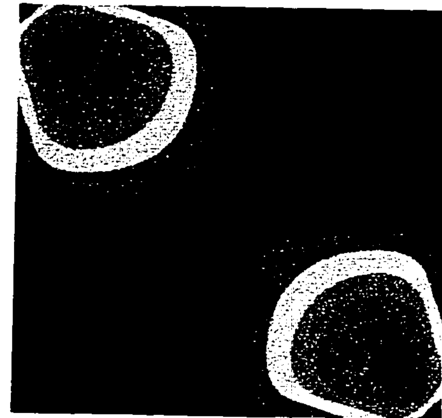
Board Thickness: 0.5 mm



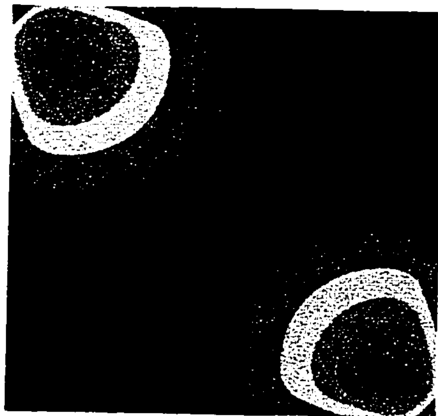
Board Thickness: 1.5 mm



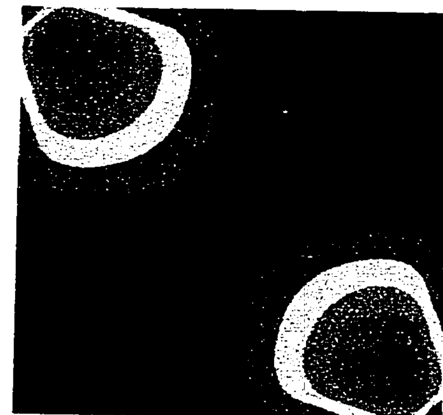
Board Thickness: 0.7 mm



Board Thickness: 2.5 mm



Board Thickness: 1.0 mm



Board Thickness: 4.5 mm

Figure 7.7 - Die Surface Stress Distribution with Varying Board Thickness
In-Plane Shear Stress (σ'_{12})

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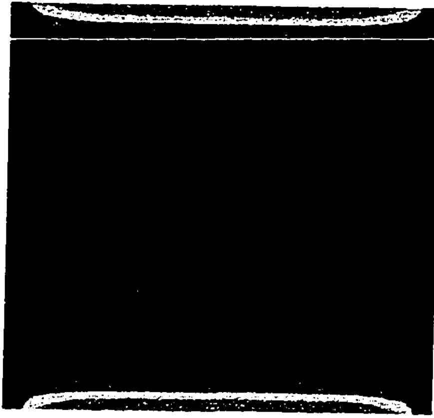
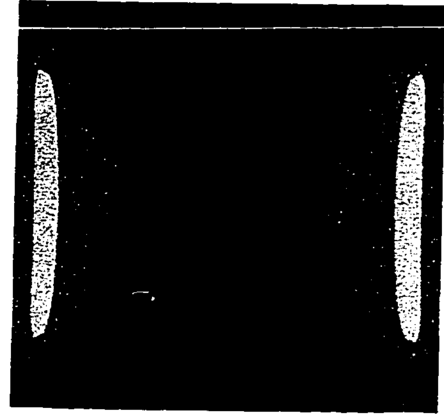
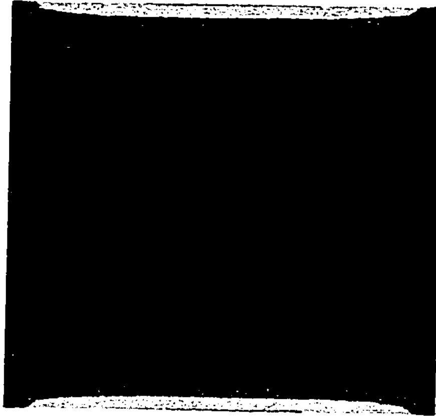


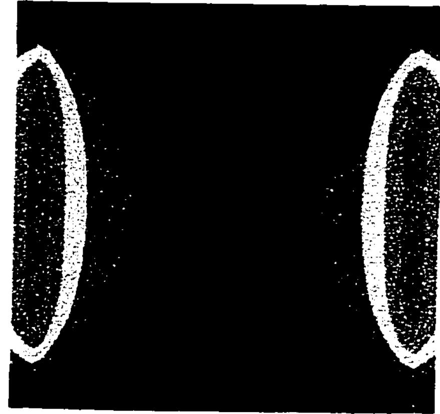
Board Thickness: 0.5 mm



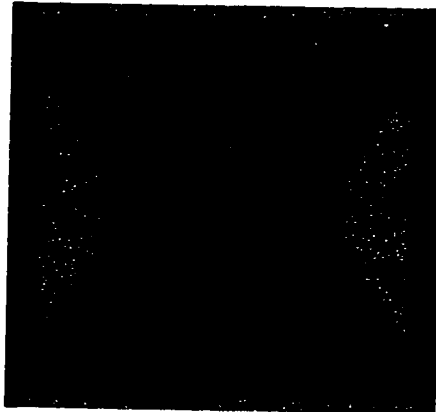
Board Thickness: 1.5 mm



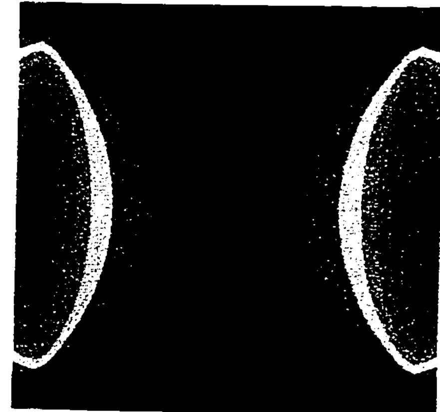
Board Thickness: 0.7 mm



Board Thickness: 2.5 mm



Board Thickness: 1.0 mm



Board Thickness: 4.5 mm

Figure 7.7 - Die Surface Stress Distribution with Varying Board Thickness
In-Plane Normal Stress Difference ($\sigma'_{11} - \sigma'_{22}$) (Continued)

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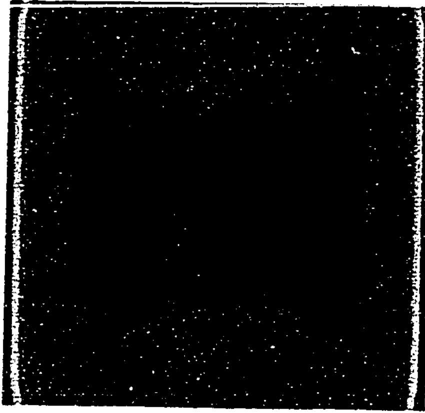
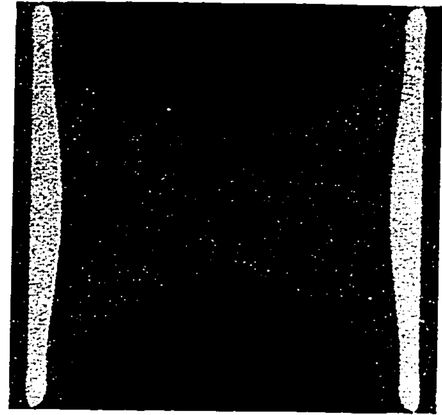
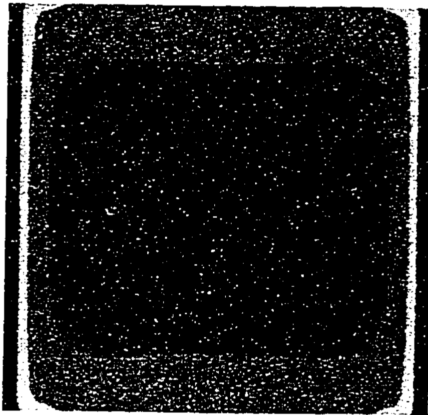


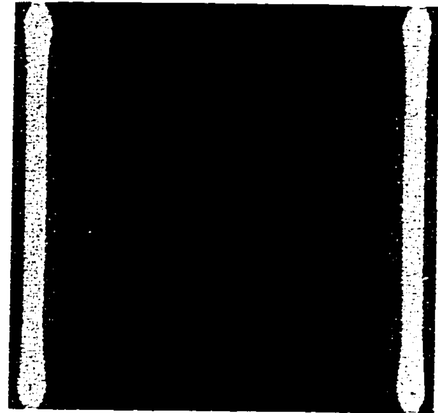
Board Thickness: 0.5 mm



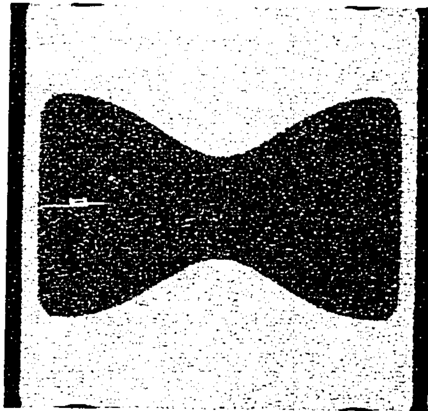
Board Thickness: 1.5 mm



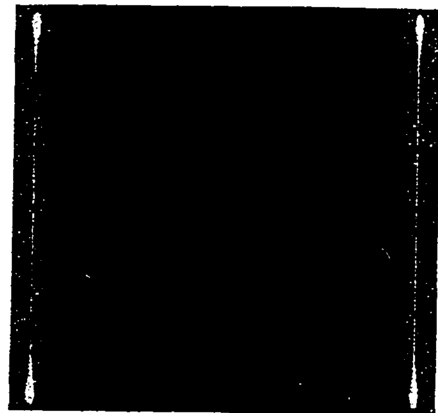
Board Thickness: 0.7 mm



Board Thickness: 2.5 mm



Board Thickness: 1.0 mm



Board Thickness: 4.5 mm

Figure 7.7 - Die Surface Stress Distribution with Varying Board Thickness
In-Plane Normal Stress (σ'_{11}) (Continued)

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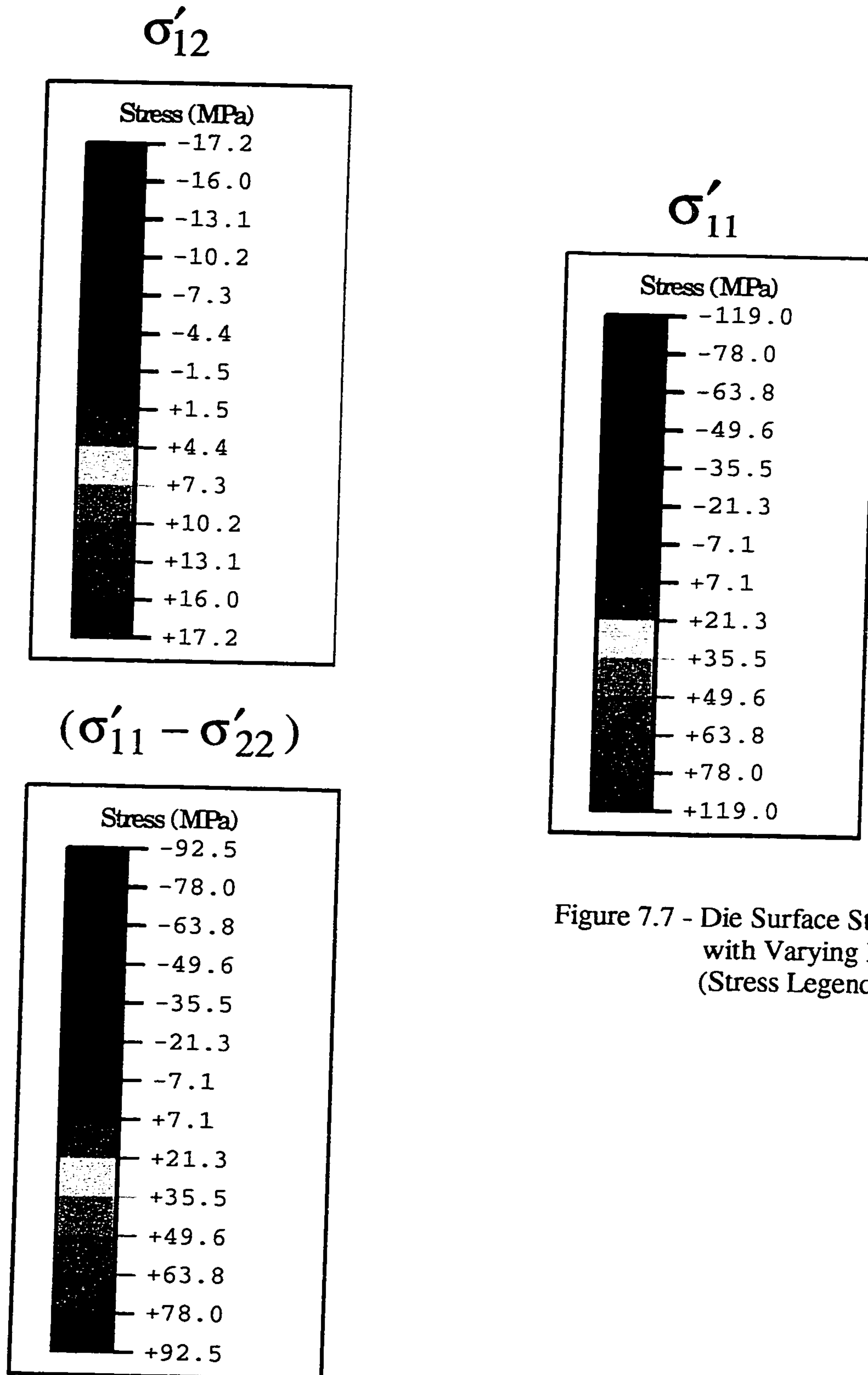

Figure 7.7 - Die Surface Stress Distribution with Varying Board Thickness (Stress Legends) (Continued)

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found when the board thickness is decreased below around 1.5 mm. As discussed above, the bending deformations may dominate the in-plane normal stress difference when the board thickness is less than 1.5 mm, while pure in-plane membrane deformations may dominate the same stress components when the board thickness is larger than 1 mm. These conclusions become obvious when considering the in-plane normal stress (σ'_{11}) variation with changing board thickness. The in-plane normal stresses in the center of the die are positive when the board is thinner, revealing that the die surface is in tension. When the board becomes thicker, the die surface stresses become compressive.

In addition to the effects of substrate thickness on the die stresses, FEM modeling was also performed to understand the contributions of the anisotropic material properties of the silicon die, and the orthotropic thermal expansion coefficients of the FR-4 board on the stress distributions on the die surface. The anisotropic material properties of silicon die were described in reference [134]. The orthotropic thermal expansion coefficients of FR-4 board were taken as: α_{11}(54e-6), α_{22}(12.8e-6), α_{33}(13.5e-6), where 1, 2 and 3 denote the directions of x'_1, x'_2, and x'_3. The other material properties in the model were taken to be the same as above. The thickness of the board was fixed at 1.5 mm. The FEM simulation results are presented in Figure 7.8. Only results for the in-plane normal stress difference on the die surface are shown. No significant changes were found when only anisotropic material properties were included for silicon die. However, significant changes were observed when orthotropic thermal expansion coefficients were adopted for the FR-4 substrate. It could be concluded that the configuration and material properties of the FR-4 board are critical for determining the magnitudes and signs of the die surface stresses

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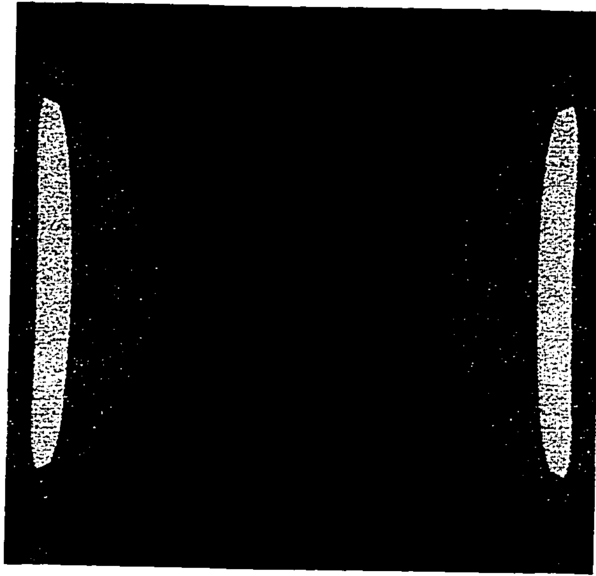
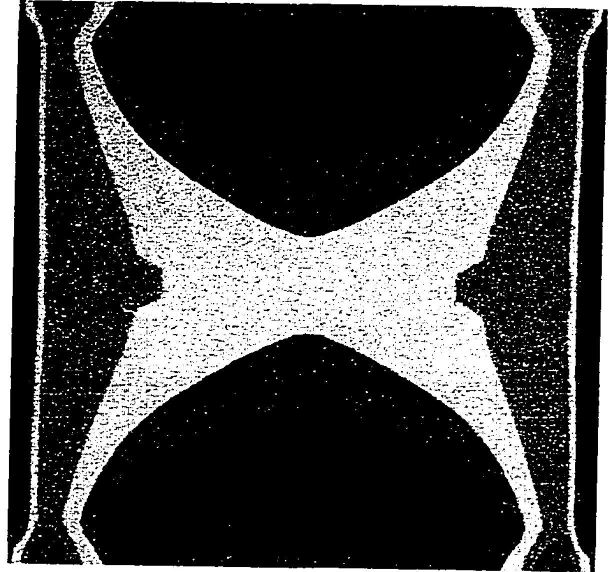
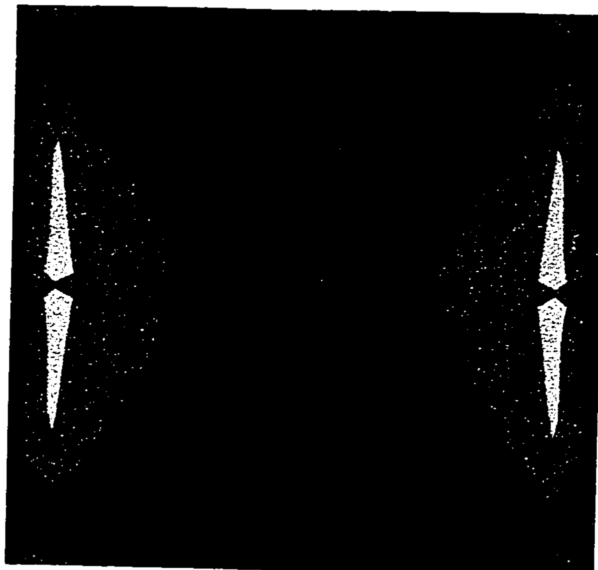


Silicon (ISO), Board (ISO)



Silicon (ANISO), Board (ORTHO)



Silicon (ANISO), Board, (ISO)

$(\sigma'_{11} - \sigma'_{22})$

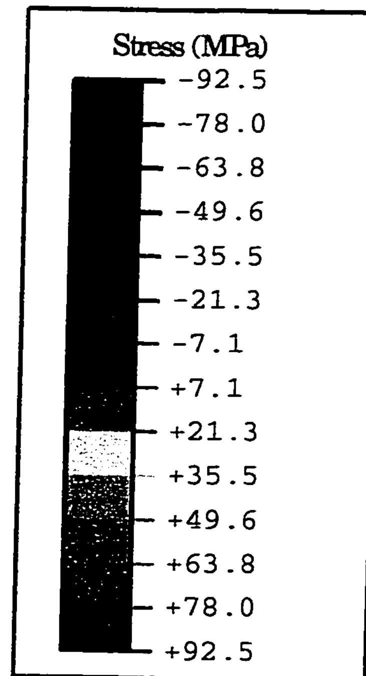


Figure 7.8 - Die Surface Stress Distribution with Varying Material Properties (ISO: Isotropic, ANISO: Anisotropic, ORTHO: Orthotropic)

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developed during COB die attachment. However, the structure of the FR-4 board may contribute much less to the die surface stresses developed during encapsulation.

To further illustrate the nature of the stresses induced by die attachment, a single COB specimen was subjected to slow temperature change from –40 °C to +140 °C. Resistance values were monitored continuously, and the stresses were extracted as a function of temperature. When using Eq. (4.4, 4.5), it was assumed that the piezoresistive coefficients were independent of temperature [123]. Typical in-plane shear stress and in-plane normal stress difference data are shown in Figure 7.9. In both cases, raising the temperature from room temperature decreases the magnitude of the stress component. As the temperature approaches 150 °C (the cure temperature of the die attachment adhesive), the stresses approach zero. Likewise, at lower temperatures the stress levels are increased. This is because the material expansion mismatch becomes worse due to the larger temperature change from the "relaxed" configuration of the package materials at approximately 150 °C.

7.4 Stresses After Encapsulation

The final stresses resulting after the encapsulant cure cycle and COB package cooling were calculated from the original (wafer level) and final (packaged) die sensor resistances, and eqs. (4.4, 4.5). Since both of these measurements and the calibration of the piezoresistive coefficients were done at room temperature (23 °C), any unexpected thermal errors will be minimized ($T = T_m - T_{ref} = 0$). Figure 7.10 shows the measured data for the in-plane shear stress σ'_{12}, in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$), and out-of-plane

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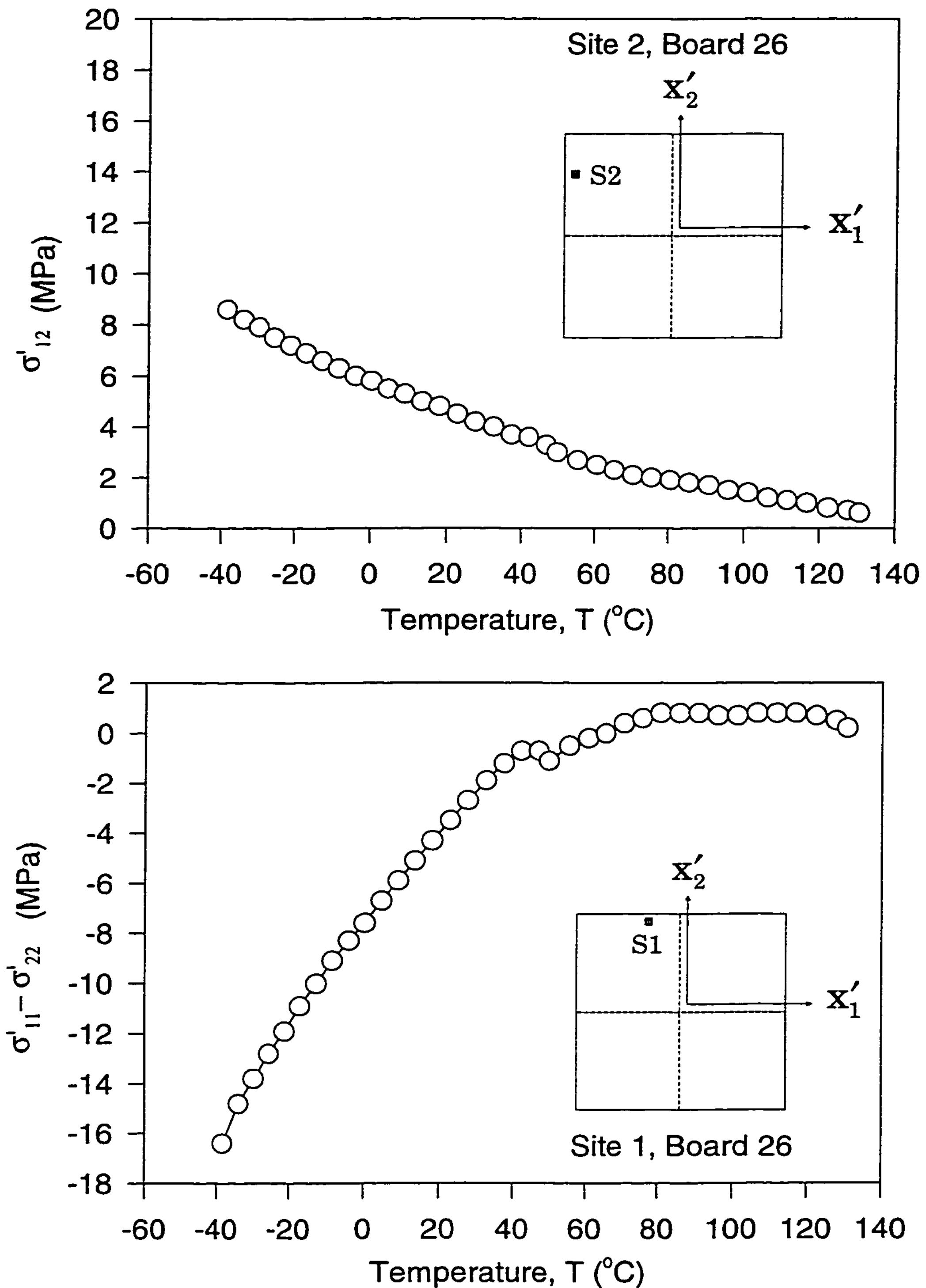

Figure 7.9 - Variation of Die Attachment Stress with Temperature (COB)

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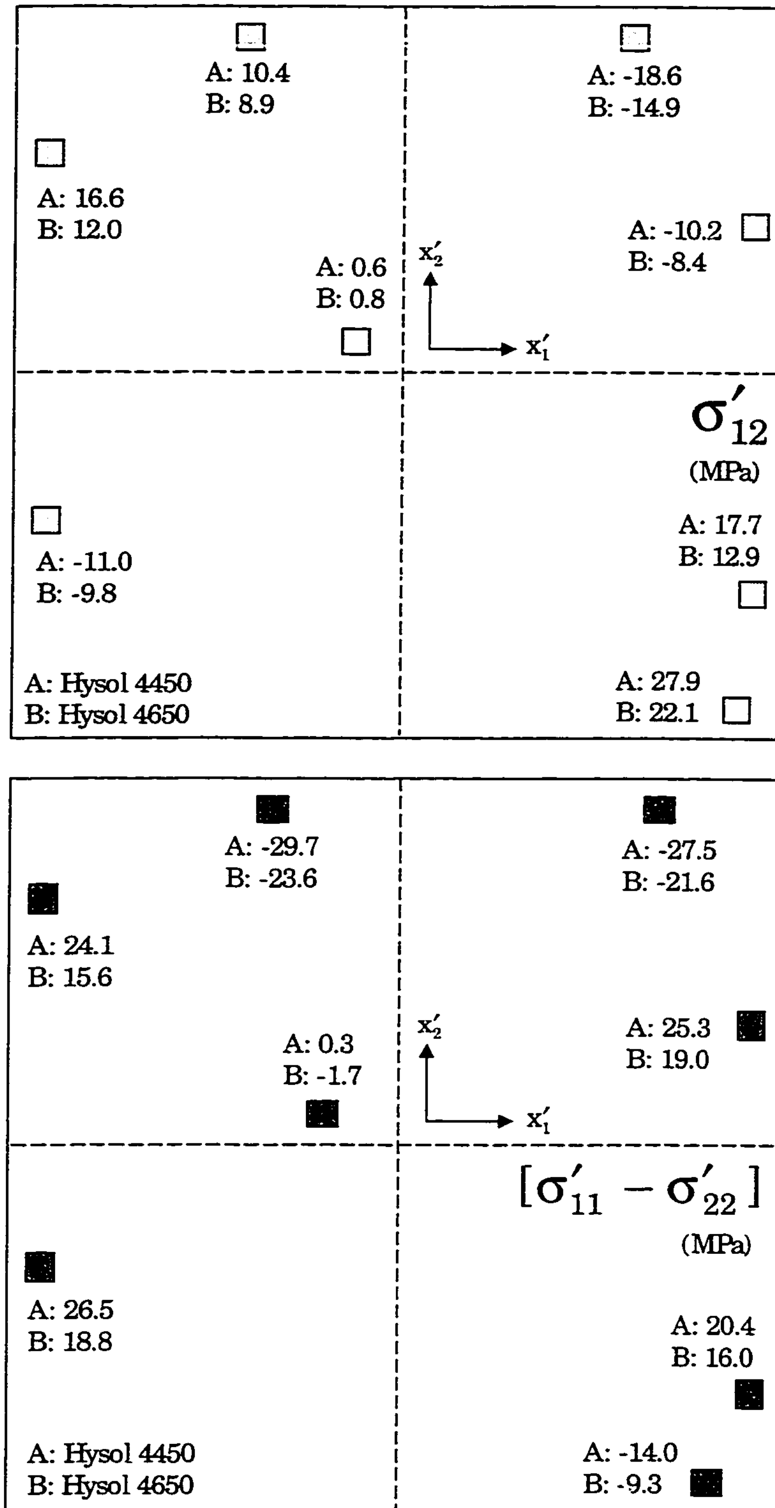

Figure 7.10 - Comparison of Measured Stresses after Encapsulation for Two Encapsulants (COB)

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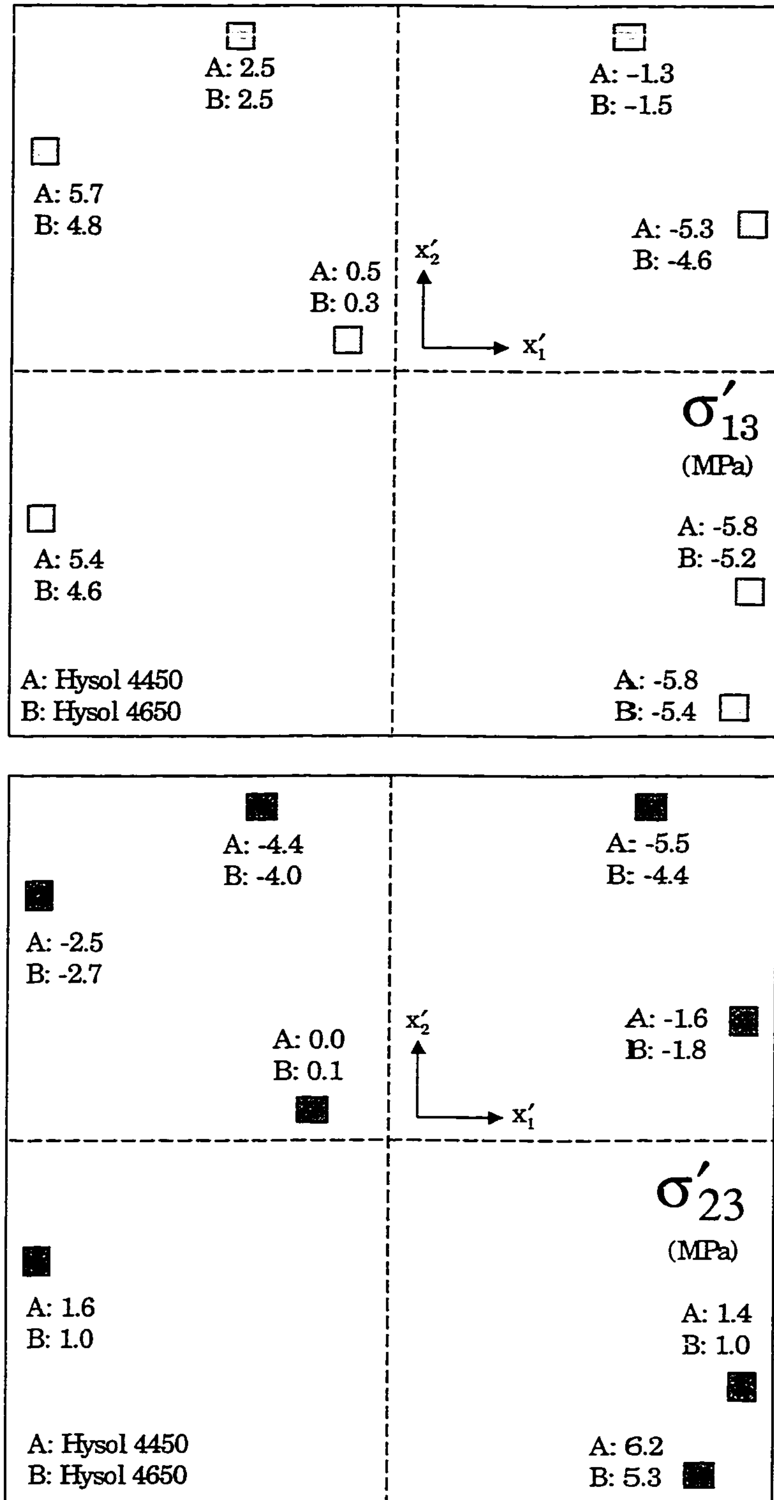

Figure 7.10 - Comparison of Measured Stresses after Encapsulation for Two Encapsulants (COB) (Continued)

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shear stresses σ'_{13} and σ'_{23}, respectively. At every rosette site in each plot, results are given for both the FP4450 and FP4650 liquid encapsulants. Each indicated value is the average of data taken from the 15 specimens used for each encapsulant.

With few exceptions, the average stress magnitudes in the FP4650 samples were smaller than those at analogous points in the FP4450 samples. The observed reductions in the in-plane die surface stresses when using the FP4650 material were typically 20-40%. The out-of-plane shear stress magnitudes are relatively small for both encapsulants when compared to the magnitudes of the in-plane stress components. Knowledge of these stress components is critical for the determination of the integrity of die/encapsulant interfaces or for the detection of interface delaminations. The recorded interfacial shear stress data for the FP4650 encapsulant were again typically reduced by 10-20% relative to the observed values for the FP4450 material. The signs of the measured stresses after encapsulation agree well with the idealized signs shown in Figure 7.5 for a plastic encapsulated package.

A single thermal cycle test was performed on a COB specimen to further illustrate the nature of the stresses induced by encapsulation (similar to the test done on one of the die attachment samples). The encapsulated COB specimen was subjected to slow temperature change from room temperature 23 °C to –50 °C. The temperature was then increased to +170 °C, and then finally reduced back to room temperature 23 °C. Resistance values were monitored continuously, and the stresses were extracted as a function of temperature. When using Eq. (4.4, 4.5), it was assumed that the piezoresistive coefficients were independent of temperature [123].

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Typical temperature compensated stress data (in-plane shear stress, in-plane normal stress difference, two out-of-plane shear stresses) for a COB sample using the Hysol FP4450 encapsulant are shown in Figure 7.11. In all cases, decreases in the stress magnitudes were observed when the temperature was raised from a low temperature extreme. As the temperature approached about 140 °C, the stresses approached zero. It should be noted that the encapsulant curing cycle was performed in two steps. After encapsulation, the COB samples were first cured at 125 °C for 30 minutes, and then subsequently cured at 165 °C for 90 minutes. The stress "relaxed" temperature of the COB samples could fall into the range of 125-165 °C. Similar to the die attachment sample testing, the die stress levels in the encapsulated specimens increased with lower temperatures. This is because the material expansion mismatch increased due to the larger temperature change from the “relaxed” configuration of the package materials at approximately 140 °C.

Abrupt changes in the stress variations were observed to occur about 140 °C. This is thought to be a result of the step changes in the CTE’s of both the die attachment adhesive and epoxy encapsulant that occur when the temperature is above their glass transition temperatures. For the die attachment adhesive, the CTE is 55 ppm/°C when the temperature is below the glass transition temperature (T_g=103 °C), and it is 150 ppm/°C when the temperature is above the T_g. While for Hysol FP4450 encapsulant, the “book value” of the CTE is 22 ppm/°C, and this is only claimed for a temperature range of 40-120 °C. A Much higher CTE value is expected for most epoxy encapsulant materials when the temperature is above their glass transition temperature. The T_g of the Hysol FP4450

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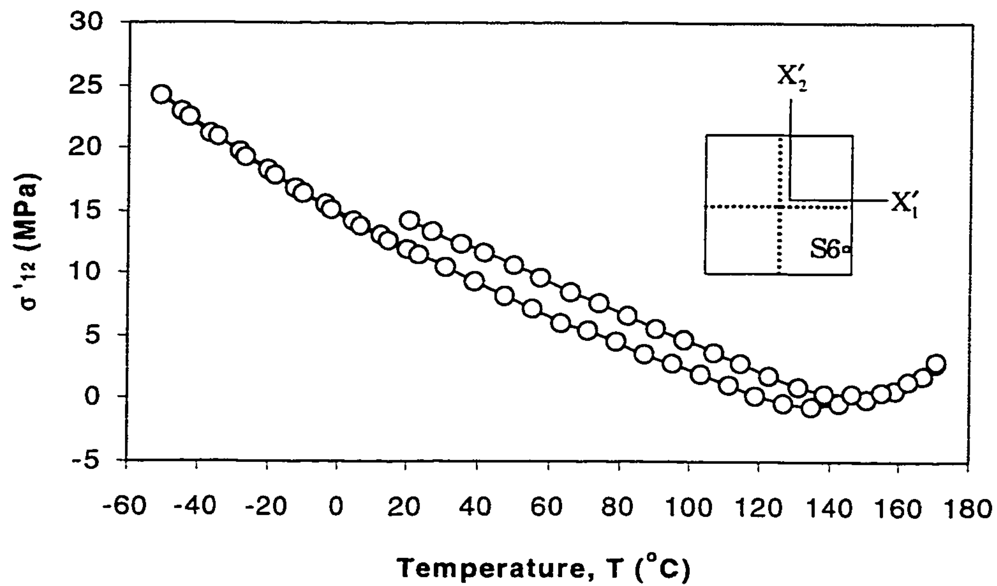

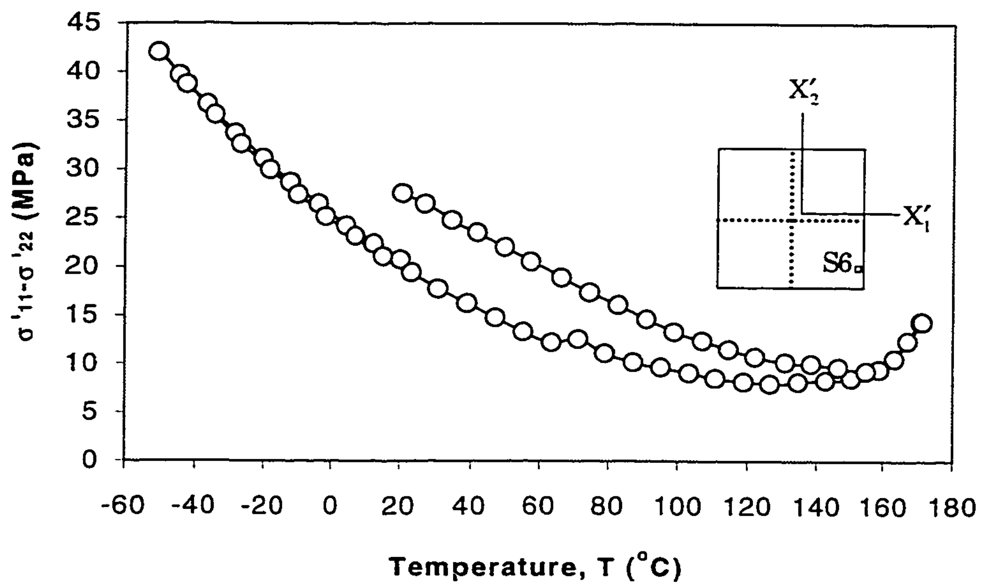

Figure 7.11 - Variation of Encapsulation Stress with Temperature (COB)

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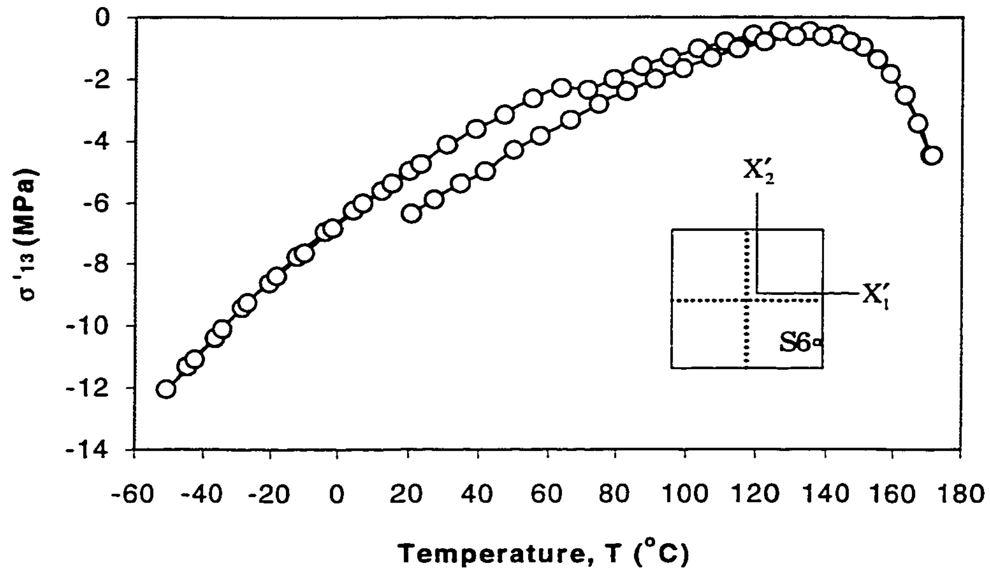

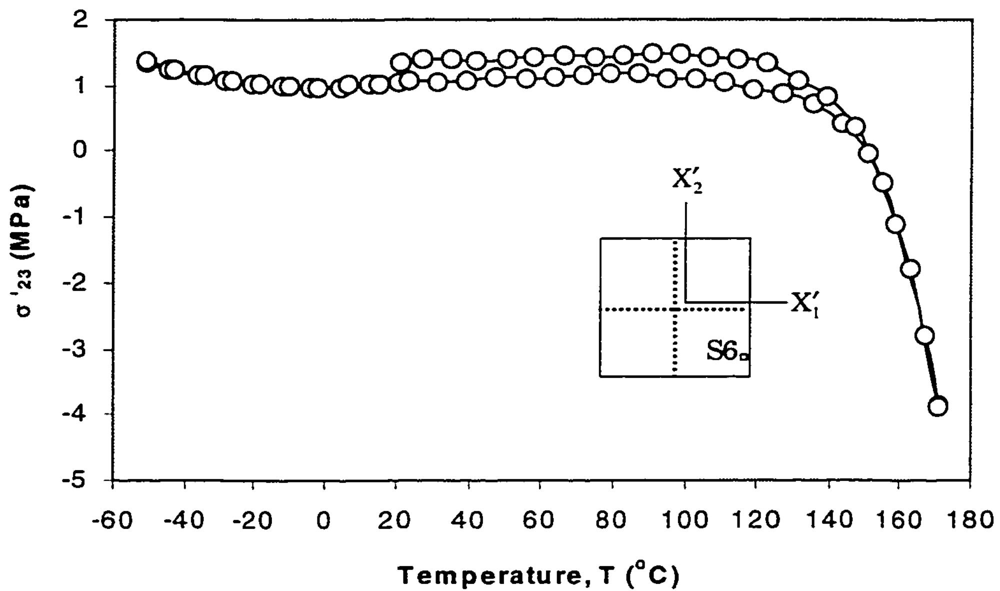

Figure 7.11 - Variation of Encapsulation Stress with Temperature (COB) (Continued)

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encapsulant is 155 °C, which is observed to be a little higher than the abrupt change point (140 °C) on the encapsulation stress variation curves. However, the temperature of 140 °C falls into between the glass transition temperature of the die attachment adhesive and the liquid encapsulant.

Finally, it is noted that stress versus temperature curves are perfectly matched for temperature increases and decreases when the temperature was changed between room temperature and -55 °C. However, stress hysteresis phenomena were observed in all of the stress components when the temperature was raised to very high levels, and then lowered. This suggests that further curing or other material changes occurred in the die attachment adhesive and liquid encapsulant.

7.5 Stress Variation During Encapsulant Cure

As mentioned previously, sensor resistances were monitored during the entire encapsulant cure process. Since the total amount of recorded data is enormous, it was chosen to present select examples here that illustrate the characteristics seen for the various rosette sites, stress components and encapsulant materials, as well as for resistors with well-matched TCRs.

In Figure 7.12, the variation of the in-plane shear stress with time is shown at site 5 (location S5 in Figure 7.3) on one of the boards encapsulated with FP4450. At time $t = 0$, the board had just been removed from the hot plate after dispensing the encapsulant, and inserted into the edge connector socket to initiate data collection. The initial shear stress value was a small positive number, and indicates the stress in the chip due to the die

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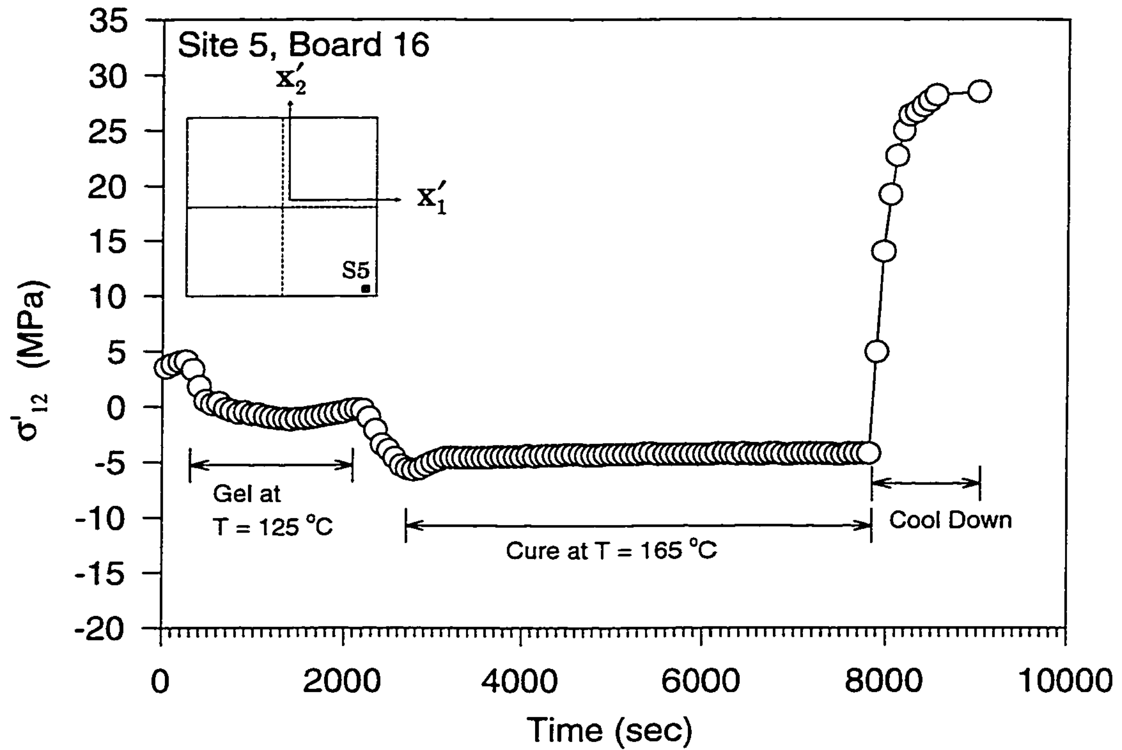

Figure 7.12 - Stress Variation During Encapsulant Cure (COB)

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attachment process (σ'_{12} = 4.5 MPa was recorded separately for this sample and site as the die attachment stress). The sample cooled slightly from the hot plate temperature of 80 °C towards room temperature during the first few hundred seconds (before putting the sample into the cure oven). This resulted in the observed slight increase in the stress magnitude (the stress became further positive). As discussed previously (see Figure 7.9), this is a consequence of the material expansion mismatch becoming worse due to the increasing temperature difference from the "relaxed" configuration of the assembly at approximately 150 °C.

The sample was inserted into the oven at approximately t = 300 sec for the gel portion of the encapsulant cure cycle. Between t = 300 sec and t = 600 sec, the sample increased in temperature and eventually reached the gel temperature of 125 °C. The sample then remained at this temperature for 30 minutes. During that isothermal period, the shear stress hovered near zero but varied slightly due to the occurrence of encapsulant shrinkage. At approximately t = 2100 sec, the oven temperature was increased to 165 °C for the second portion of the encapsulant cure cycle. As the temperature of the sample increased, the shear stress became more and more negative due to the thermal expansion mismatch of the assembly materials. In this case, the observed variation resulted from a complicated combination of a fully cured die attach material and partially cured encapsulant. However, the trend continued where the stress became further negative as the temperature increased.

During the hold at 165 °C, the variation of the shear stress reversed direction and started reducing slightly in magnitude, heading back towards zero. This was especially true during the first few hundred seconds of the secondary cure, suggesting that most

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encapsulant shrinkage occurs almost immediately at the 165 °C cure temperature. It should be noted that the oven temperature did not overshoot during these measurements. Upon completion of the 90 minute hold at 165 °C, the board was removed from the oven and allowed to cool in a room temperature environment. As seen from Figure 7.12, the majority of the final stress in the die was developed during this cool down period, where the encapsulant is fully hardened and can provide a significant stiffness to stress the low CTE silicon die material. Within approximately 1000 seconds, the shear stress became constant at a value of $\sigma'_{12} = 28.5$ MPa.

It is clear that the events during the cure cycle are quite complicated. However, the type of behavior shown in Figue 7.12 and discussed above was quite typical. As another example, the variation of the in-plane normal stress difference with time is also shown in Figure 7.13 at site 2 (location S2 in Figure 7.3) on the same board. Similar arguments can be made to explain the observed phenomena.

As discussed earlier (section 4.2.3), a total temperature change of 150 °C would result in measurement errors of less than 7 MPa for $(\sigma'_{11} - \sigma'_{22})$ and of less than 3.5 MPa for σ'_{12}. The maximum error estimates are even smaller for the out-of-plane shear stresses. Thus, in Figure 7.12 for example, less than 10% of the 35 MPa change in shear stress observed during cool down could be attributable to resistor TCR mismatch using even a highly pessimistic estimate. Likewise, less than 10% of the change in stress that occurs in going from the gel temperature to the cure temperature can be due to errors from TCR mismatches. It is worth mentioning that not all sensors give such good results as those

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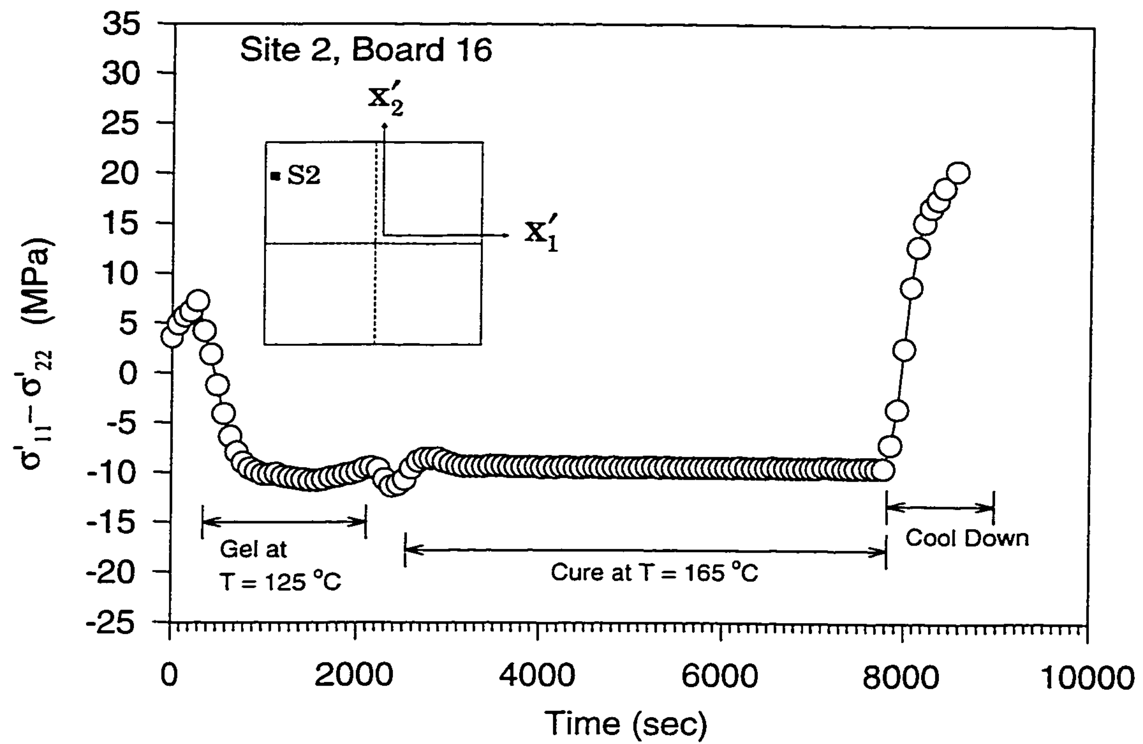

Figure 7.13 - Stress Variation During Encapsulant Cure (COB)

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shown in Figure 7.12, and it can easily be deduced from the data when a resistor pair has poorly matched TCRs.

7.6 Finite Element Simulation

The final room temperature experimental results for encapsulant A (Hysol FP4450) have been evaluated through correlation with the predictions of nonlinear three-dimensional finite element simulations of the packaging process. In the finite element models, the materials were modeled as linear elastic. Temperature dependent mechanical properties and large deformations (kinematic nonlinearities) were utilized. The time dependent (viscoelastic) behavior of the liquid encapsulant was neglected to simplify the analysis, and because of a lack of material characterization data needed to generate an accurate constitutive model for the encapsulant. A quarter model of the specimen volume near the chip was meshed (see Figure 7.14). Figure 7.15 depicts the COB sample dimensions used in the FEM simulations. The temperature dependent material properties of the Hysol FP4450 encapsulant are listed in Table 7.2. All of the other material properties were listed in section 7.3. The die was assumed to be stress free at the glass transition temperature of the filled epoxy encapsulant, and cooling from the glass transition temperature to room temperature was simulated.

There were several limitations in the finite element simulation. The elastic modulus of the encapsulant and die attachment adhesive were experimentally obtained. However, data for the Poisson's ratios and coefficients of thermal expansion were not available, so they were assumed to be temperature independent. The "stress free" state of package is hard

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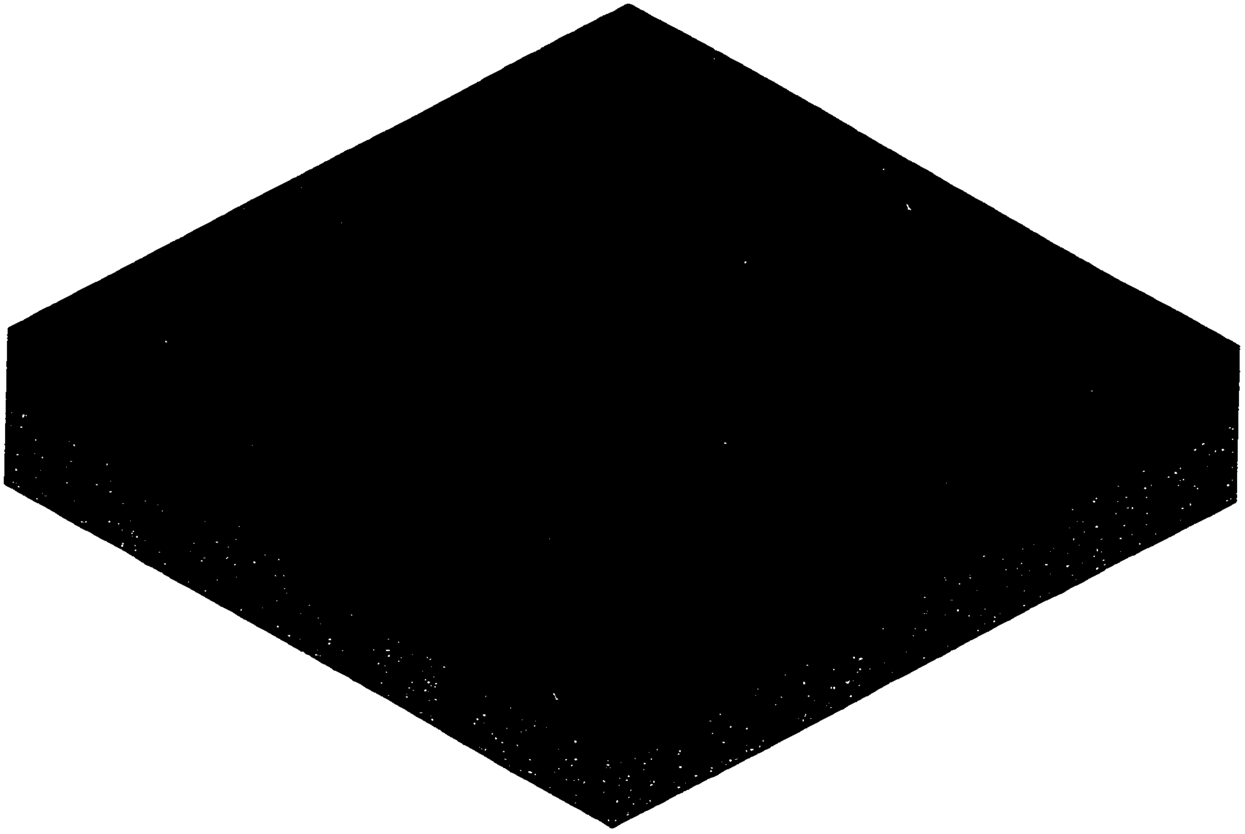

Figure 7.14 - COB Finite Element Mesh (One Quarter Model Near the Die)

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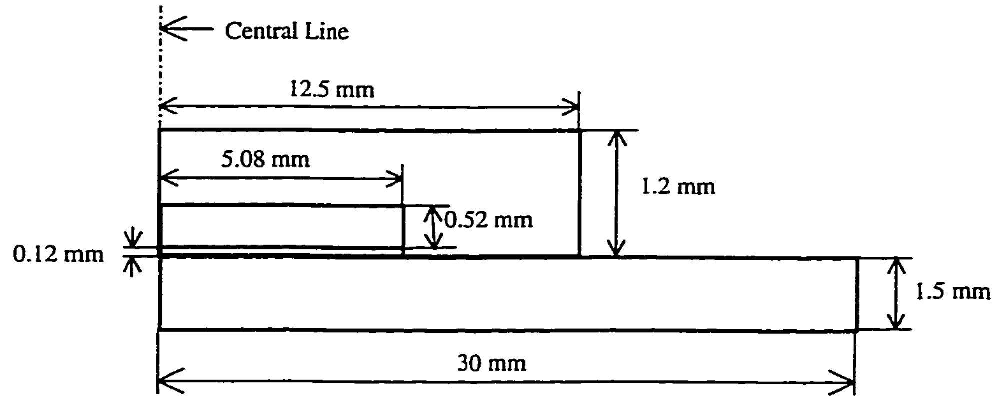

Figure 7.15 - Dimensions of COB Encapsulation Model

Materials	E (GPa)	α (ppm/°C)	ν	T_g (°C)
Encapsulant (-50°C)	9.7	22	0.4	155
Encapsulant (-25°C)	9.43	22	0.4	155
Encapsulant (0°C)	9.1	22	0.4	155
Encapsulant (25°C)	8.73	22	0.4	155
Encapsulant (30°C)	8.66	22	0.4	155
Encapsulant (40°C)	8.53	22	0.4	155
Encapsulant (50°C)	8.33	22	0.4	155
Encapsulant (60°C)	8.20	22	0.4	155
Encapsulant (70°C)	8.06	22	0.4	155
Encapsulant (80°C)	7.90	22	0.4	155
Encapsulant (90°C)	7.76	22	0.4	155
Encapsulant (100°C)	7.56	22	0.4	155
Encapsulant (110°C)	7.26	22	0.4	155
Encapsulant (120°C)	6.83	22	0.4	155
Encapsulant (130°C)	6.20	22	0.4	155
Encapsulant (140°C)	5.46	22	0.4	155
Encapsulant (150°C)	4.6	22	0.4	155
Encapsulant (160°C)	3.5	22	0.4	155
Encapsulant (170°C)	2.16	22	0.4	155

Table 7.2 – Hysol FP4450 Properties

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to identify when considering both curing cycles for the die attachment adhesive and the encapsulant. Thus, a model consisting of cooling down from 155 °C, the glass transition temperature of FP 4450, is not exact. In addition, perfect bonding was assumed at all the interfaces of dissimilar materials. These assumptions will affect the precision of the FEM modeling. Finally, linear elastic behavior was assumed for all the packaging materials, which will contribute to additional FEM simulation errors. It is well known that epoxy molding compounds usually exhibit viscoelastic or viscoplastic characteristics at high temperatures.

It should be emphasized that the experimental measurements were the main emphasis of this work. The finite element model predictions were used to show the proper signs and approximate trends of the various stress component distributions, so that the experimental data could be better understood. In addition, correlation of the finite element predictions with the test chip data allowed for identification of the limitations of using an expedient but approximate engineering numerical simulation procedure which neglects encapsulant relaxation.

Figure 7.16 illustrates temperature compensated experimental measurements and finite element predictions for the die surface distributions of the in-plane shear stress σ'_{12}, in-plane normal stress difference (σ'_{11} - σ'_{22}), and the out-of-plane shear stresses σ'_{13} and σ'_{23}, respectively. In these plots, the colored contours are the room temperature stress distributions predicted by the finite element model. Each of the small squares in these diagrams locates a sensor rosette site. The color of a given square represents the average

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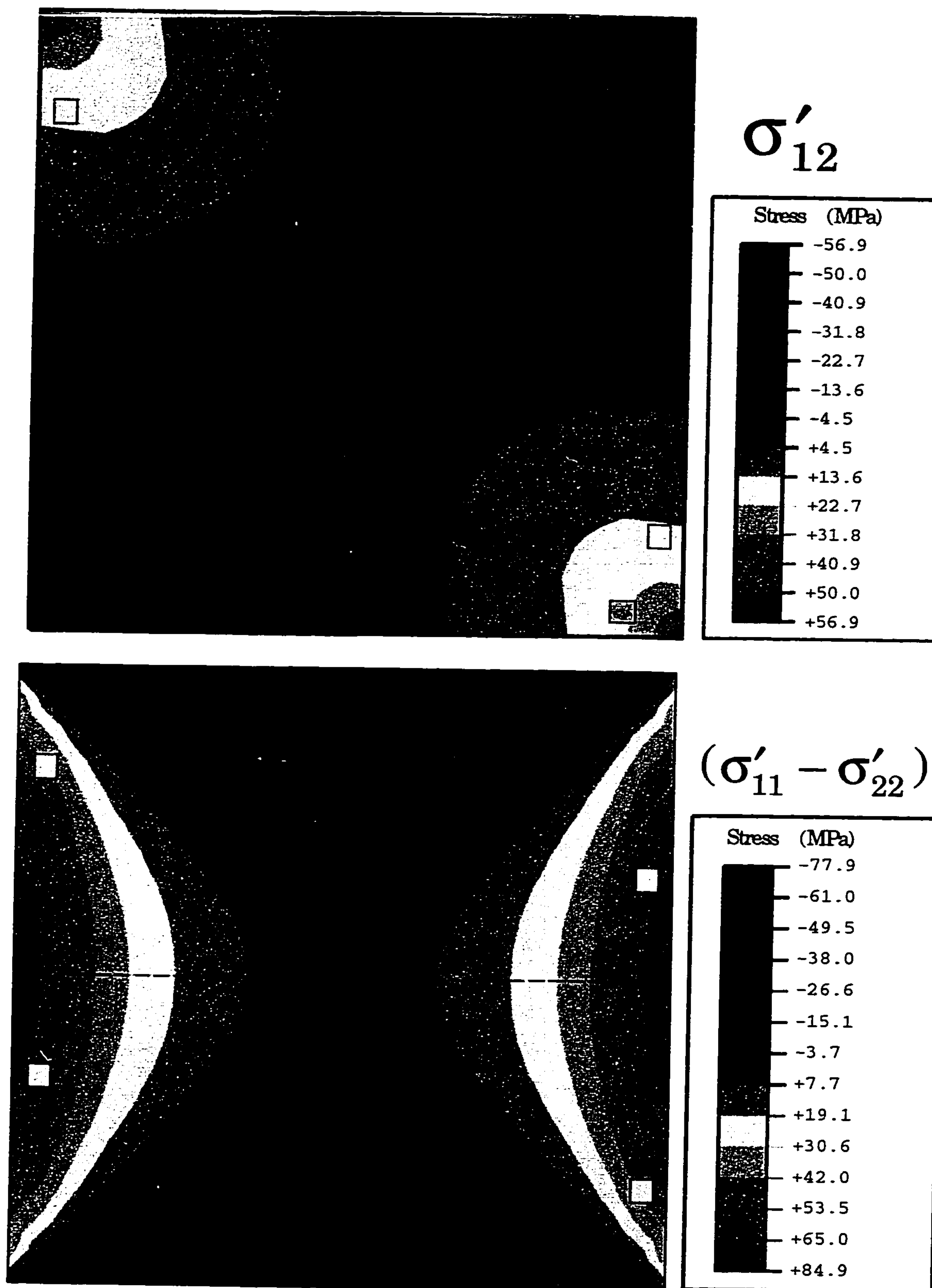

Figure 7.16 - Finite Element Contours and Experimental Data (COB)

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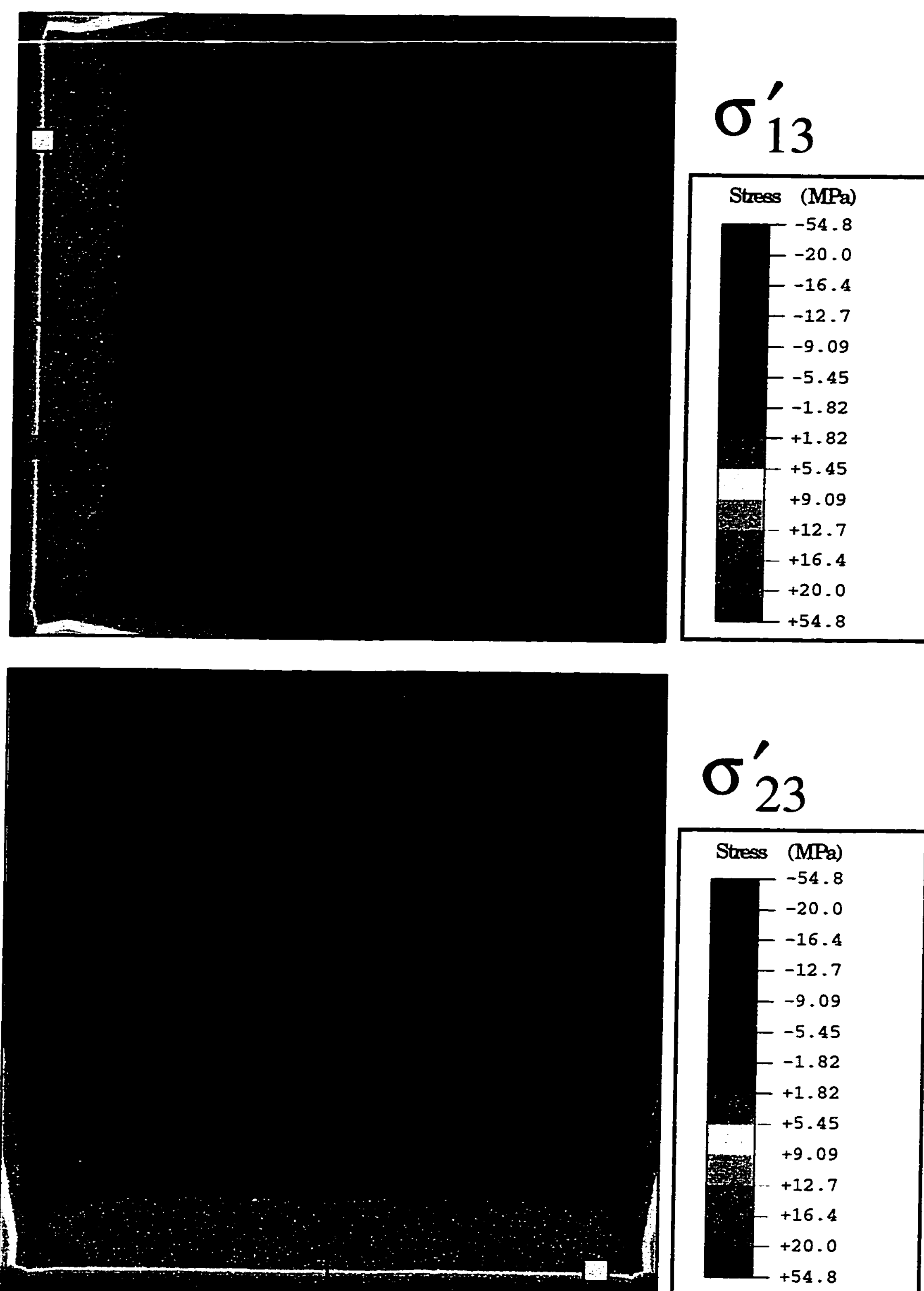

Figure 7.16 - Finite Element Contours and Experimental Data (COB) (Continued)

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room temperature experimental value of the stress at the rosette site, when considering the results for all 15 specimens (the square is colored to the same scale/legend of the finite element contours). These experimental data are the same as shown in Figure 7.10 for the FP4450 encapsulant.

It can be see that the finite element predictions are in reasonable agreement with the experimental results. The measured stresses show the same trends and numerical signs as the distributions predicted by finite element analysis. The correlations of the experimental and numerical shear stress values are excellent. However, the finite element model over predicts the observed normal stress difference data since the viscoelastic relaxation of the filled epoxy encapsulant was neglected. This demonstrates the valuable role that test chip data can fill as a verification tool for the assumptions made in numerical modeling techniques.

7.7 Summary

In this work, (111) silicon test chips have been used to characterize the variation of die stress throughout the COB packaging process. The initial sensor resistances were recorded when the test die were in wafer form. The rosettes were later characterized after die attachment, and throughout the cure cycle of the liquid encapsulant. Using the measured data and appropriate theoretical equations, the stresses at sites on the die surface have been calculated. Die stresses due to the die attachment process were shown to be relatively small. In addition, these stresses approached zero as the specimens were heated back up to the cure temperature of the die attachment adhesive. The stress "relief"

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phenomenon near the curing temperature of encapsulant were also verified when the COB samples were subjected to changing temperatures. The observed stress variations during the encapsulant cure cycle were quite complicated. Stresses were small during the encapsulant gel at 125 °C, and most of the encapsulant shrinkage was observed to occur at the beginning of the 90-minute cure at 165 °C. The majority of the final stresses in the packaged die were developed during the cool down period after the encapsulant cure cycle. The observed room temperature stress distributions followed expected trends. Two encapsulants were utilized, and a consistent reduction of the die stress magnitudes was observed when using the "low stress" encapsulant material (with lower CTE). Up to 40-50% reductions in the magnitudes of certain stress components were observed.

Three-dimensional nonlinear finite element simulations of the chip on board packages were also performed, and the stress predictions were correlated with the room temperature experimental test chip data. The experimental shear stress results were in good agreement with the finite element predictions. However, improvement in the constitutive model for the filled epoxy encapsulant will further improve the finite element predictions of the normal stress distributions.

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CHAPTER 8

COMPARISON OF CHIP-ON-BOARD STRESS LEVELS WITH CONVECTION AND VARIABLE FREQUENCY MICROWAVE ENCAPSULANT CURING

8.1 Introduction

Liquid encapsulation of semiconductor devices continues to grow in both single chip and chip-on-board (COB) assembly. The industry trends of larger die and thinner laminates pose challenges to encapsulation. Increasing die sizes lead to increased stresses at the die-to-encapsulant interface, while thinner laminates result in increased substrate warpage. Excessive die stresses can result in delamination or fracture of the silicon die. Warpage leads to problems at the next level of assembly.

To address stress and warpage issues, new generations of liquid encapsulants are being formulated which have low shrinkage during curing and low coefficients of thermal expansion (CTE). In addition, longer cure cycles are being recommended to minimize warpage. Such longer cure times (typically 5-7 hours) translate to more work-in-progress, longer cycle times, and delays in process feedback.

Variable frequency microwave (VFM) processing has been developed as an alternative to convection curing. In recent work, VFM techniques have been shown to significantly reduce epoxy curing times [135, 136]. In this work, die level stresses are

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compared for COB packages processed using convection and VFM curing. The substrate warpages with respect to the same COB packages are discussed in reference [121].

Using special (111) oriented silicon stress test chips, the die surface stress due to encapsulation was measured for a commercial encapsulant cured with both convection and VFM curing. The test die contained an array of optimized sensor rosettes that are capable of evaluating the complete stress at points on the surface of the die. Stresses were monitored in-situ during the convection cure cycle. However, microwave interference with the measurement signals did not permit in-situ monitoring for the VFM cure. A comparison was made between the room temperature stresses found with each method of curing. After cure, the samples from each curing method were divided into two groups, and reliability tests were performed. The first group of samples was subjected to thermal cycling over the range of –40 °C and +125 °C. The second group was exposed to high humidity storage at 85% RH and 85 °C. In each case, changes in the die stress levels were monitored for samples from each curing method to detect delaminations due to thermal cycling and to study the impact of moisture absorption. Finally, a comparison of the stresses introduced at the FR-4 board level for each curing method was made through substrate warpage measurements (see reference [121]).

8.2 COB Packaging Studies

The BMW-2 stress test chips used in this study had dimensions of 400 x 400 x 20 mils or 10.2 x 10.2 x .5 mm (2 x 2 array of the die schematic shown in Figure 4.8). FR-4 printed circuit board (PCB) test vehicles were prepared with dimensions of 12.7 cm x

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10.74 cm x 1.1 mm, and with one central die bond site. The printed circuit board was designed using Lavenir software, and Figure 8.1 shows the layout of the PCB design. The PCB used in this study was of higher density than the board discussed in the previous chapter, and four more rosettes could be monitored on the same test chip. The test die were bonded to the FR-4 substrates using a silver-filled epoxy die attachment adhesive (Ablestik Ablebond 84-1LMI). Thermosonically bonded gold wires were then used to provide the interconnections from the die bond pads to the metal traces on the PCB's. Finally, the test chips were encapsulated using an epoxy liquid encapsulant (dam and fill process). A total of 24 specimens were prepared. The liquid encapsulant applied to the samples was then cured using either convection or VFM cure processes (12 samples were cured with each of the two methods). A schematic of the COB test specimen geometry is illustrated in Figure 7.1.

Although there are 20 accessible rosette sites on the 400 x 400 mil BMW-2 test die, only twelve were utilized in this study due to line width and routing limitations on the PCB. The copper traces on the PCB were routed to the edge of the board, and a standard edge connector was used to provide electrical connection of the samples to a data acquisition system. Figure 8.2 shows the selected rosette sites for stress measurement.

Before packaging, the initial room temperature resistances of all of the sensors were recorded when the chips were in wafer form using an automated probe station. The characterized test die were then diced from the wafers and bonded to the PCB's. After die attachment and wire bonding, the sensor resistances were again measured. Finally, the

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Figure 8.1 - PCB Design for Chip-on-Board Package

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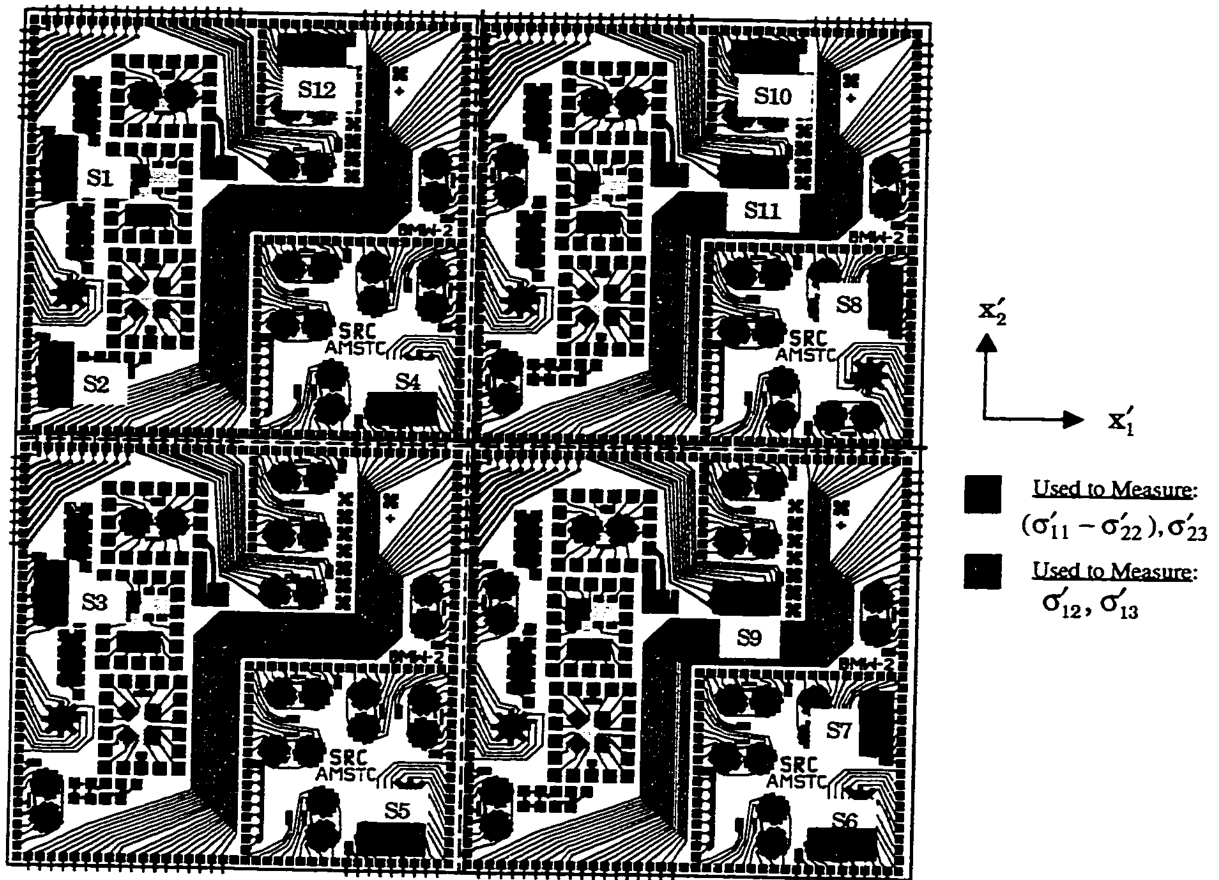

Figure 8.2 - Sensor Rosette Locations (400 x 400 mil Chip)
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liquid encapsulant materials were applied and the samples were cured with the two types of ovens.

The chips were encapsulated using a dam (Dexter Hysol FP4451) and fill (Dexter Hysol FP4651) approach. A Camalot 3600 Dispenser with a 680 PDP positive displacement pump was used for dispensing the materials. The under-board heating stage was set to 70 °C, and a spiral pattern was used to dispense the fill material.

For the specimens processed using a conventional convection cure, a Blue M oven was used. The convection cure profile was 2 hours at 110°C, followed by 3 hours at 165°C (5 hours total). After removal from the cure oven, the samples were cooled to a normal room temperature environment of 23 °C. Transient sensor resistances were monitored during the entire encapsulant cure process, and the post packaging room temperature resistances of the sensors were recorded.

For the specimens processed using variable frequency microwave curing, a MicroCure 5100 in-line system manufactured by Lambda Technologies was utilized. The cure profile as measured by IR pyrometry is shown in Figure 8.3. This profile consisted of 5 minutes at 110 °C, 5 minutes at 120 °C, 5 minutes at 130 °C, and 20 minutes at 165 °C (35 minutes total). An attempt was made to monitor the sensor resistances (stress) during the cure process. However, interference of electromagnetic energy with the measurement signals resulted in too much electrical noise for valid measurements. Thus, for the VFM cured specimens, only the post packaging room temperature stresses after cure cool down will be reported.

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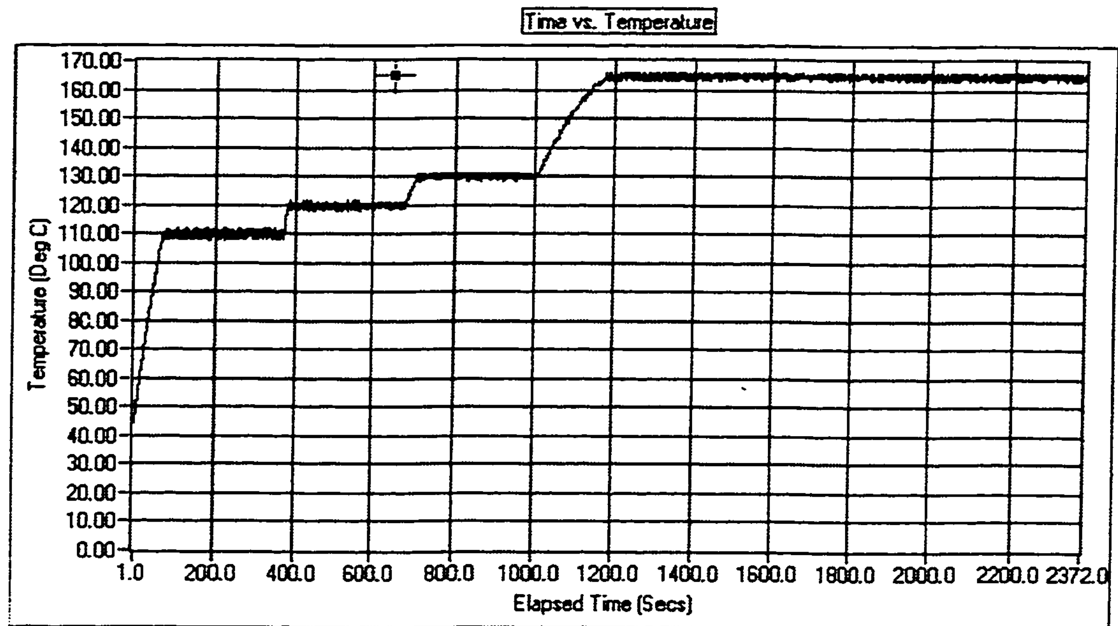

Figure 8.3 - VFM Curing Profile

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After curing and cool down, stress variations in the final packaged die were measured as a function of temperature from -40 °C to +140 °C. Also, the 12 samples from each curing method were divided into two groups of 6, and reliability tests were performed. The first group of samples was subjected to thermal cycling between –40 °C and +125 °C. The second group was exposed to high humidity storage at 85% RH and 85 °C. In each case, changes in the die stress levels were monitored for samples from each curing method to detect delaminations due to thermal cycling and to study the impact of moisture absorption.

8.3 Stress Due to Die Attachment

After the test chips were bonded to the FR-4 substrates, the die attachment adhesive was convection cured for 60 minutes at 150 °C per vendor instructions. The specimen assemblies were then cooled to room temperature and the thermosonic gold wire bonding was performed to interconnect the perimeter bond pads on the die to the substrate traces. Sensor resistances were recorded, and the die surface stresses induced by the die attachment process were calculated using these measurements and the resistance data recorded while the die were still in wafer form. At the die attach cure temperature, the adhesive is fairly relaxed/uncured and the die is nearly stress free. When the assembly is cooled down to room temperature, thermal stresses are generated in the die due to the differential shrinkages resulting from the differences in the coefficients of expansion of the die ($\alpha = 2.3 \times 10^{-6}$ 1/°C), the die attachment adhesive ($\alpha = 55 \times 10^{-6}$ 1/°C), and the FR-4 substrate ($\alpha = 15 \times 10^{-6}$ 1/°C).

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The measured values of the in-plane shear stress σ'_{12} and the in-plane normal stress difference (σ'_{11} - σ'_{22}) are shown in Figure 8.4. Each indicated value is the average of data taken from the entire set of 24 specimens. The magnitudes are universally small when compared to the stresses typically induced by topside encapsulation, where the sensor surface is contacted directly by a material of drastically different CTE. The signs of the measured normal stress difference values are in contrast to those presented in Chapter 7. This was due to the relatively thin substrate used in this study, and the different orthotropic material properties of the substrate. The effects of board thickness and board orthotropic material properties on the die surface stresses have also been discussed in Chapter 7. The average measured magnitudes of the out-of-plane shear stresses σ'_{13} and σ'_{23} were typically less than 1 MPa, a level that approaches the resolution limit of the experimental method. Note that these shear stresses are theoretically zero at this point in the packaging process, due to the fact that the die surface is still free of shear tractions.

8.4 Stress Variation During Encapsulant Cure

As mentioned previously, transient sensor resistances were monitored during the entire encapsulant cure process for the specimens cured in the convection oven. Typical data are illustrated in Figures 8.5-8.8. In Figure 8.5, the variation of the in-plane shear stress (σ'_{12}) with time and temperature is shown for site 10 (location S10 in Figure 8.2). In Figures 8.6 and 8.8, the variations of the in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$) and the out-of-plane shear stress (σ'_{23}) with time and temperature are shown for site 5 (location

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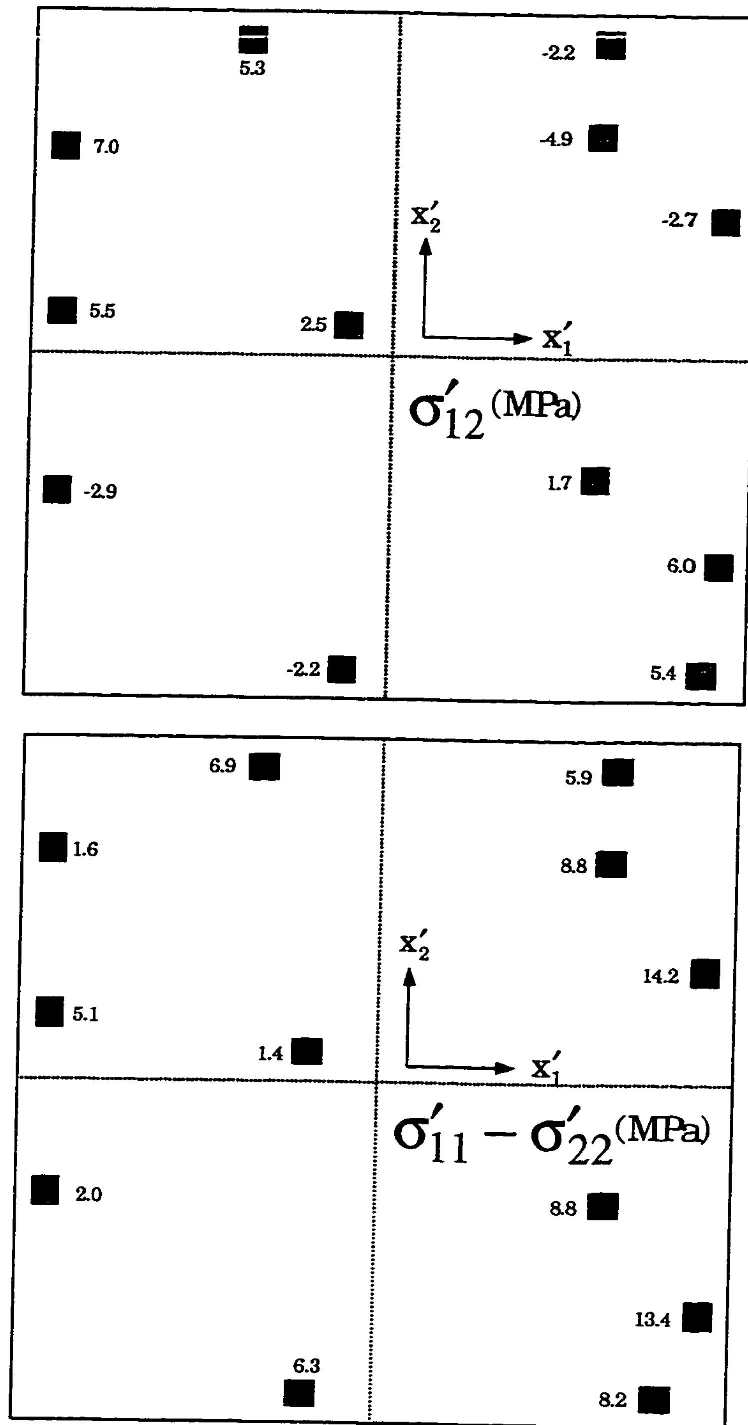

Figure 8.4 - Measured Stresses after Die Attachment
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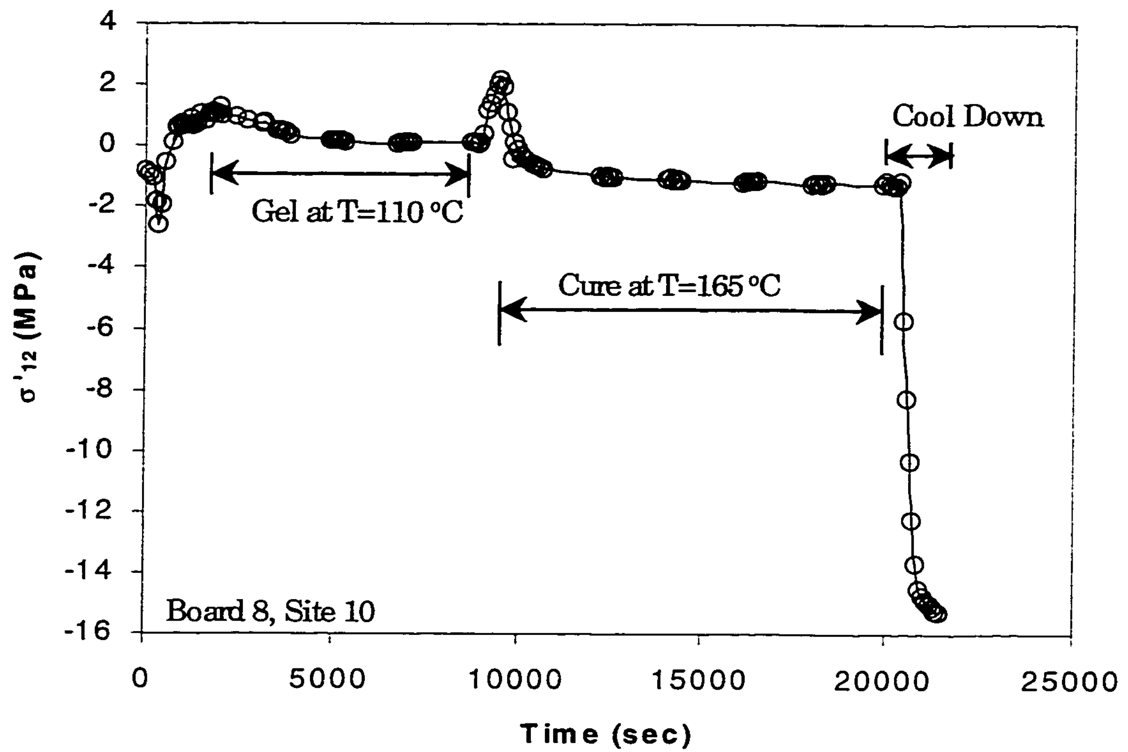

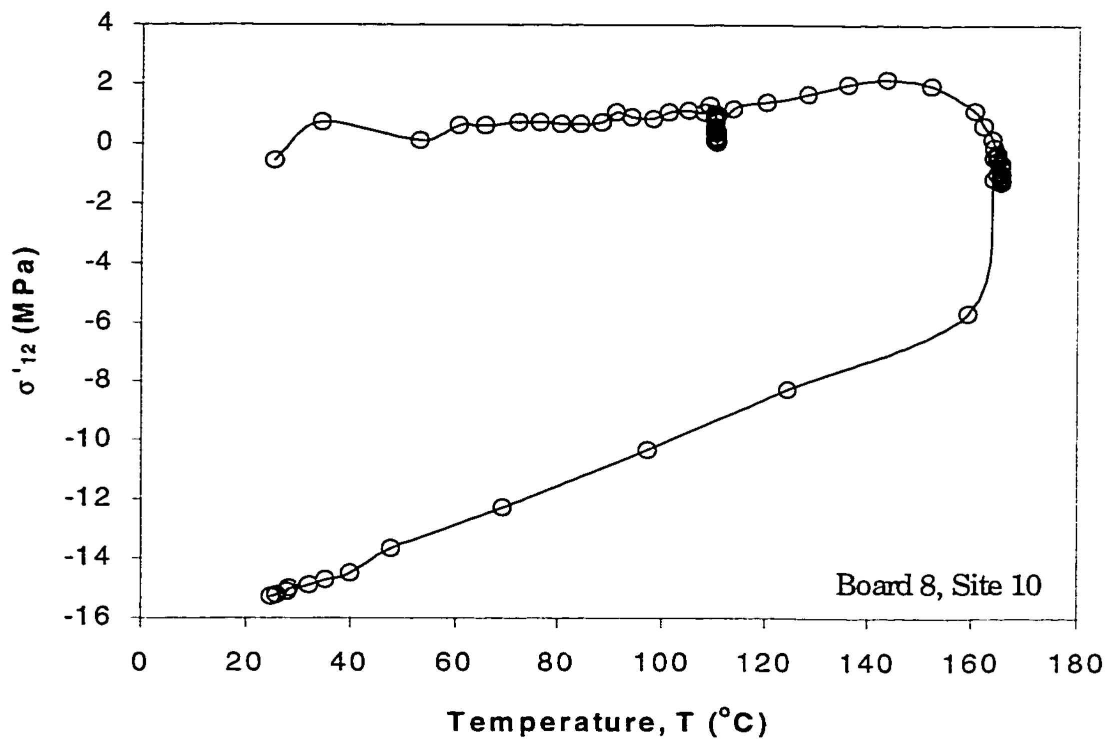

Figure 8.5 - Stress Variation During Convection Cure (σ'_{12})
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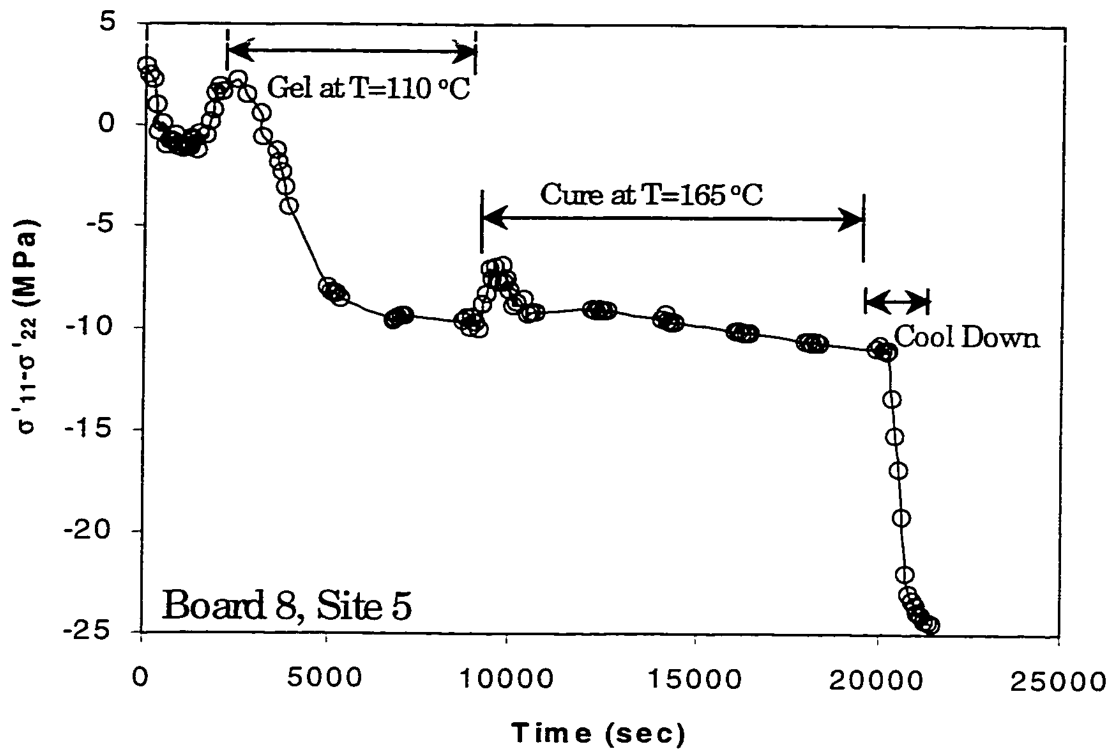

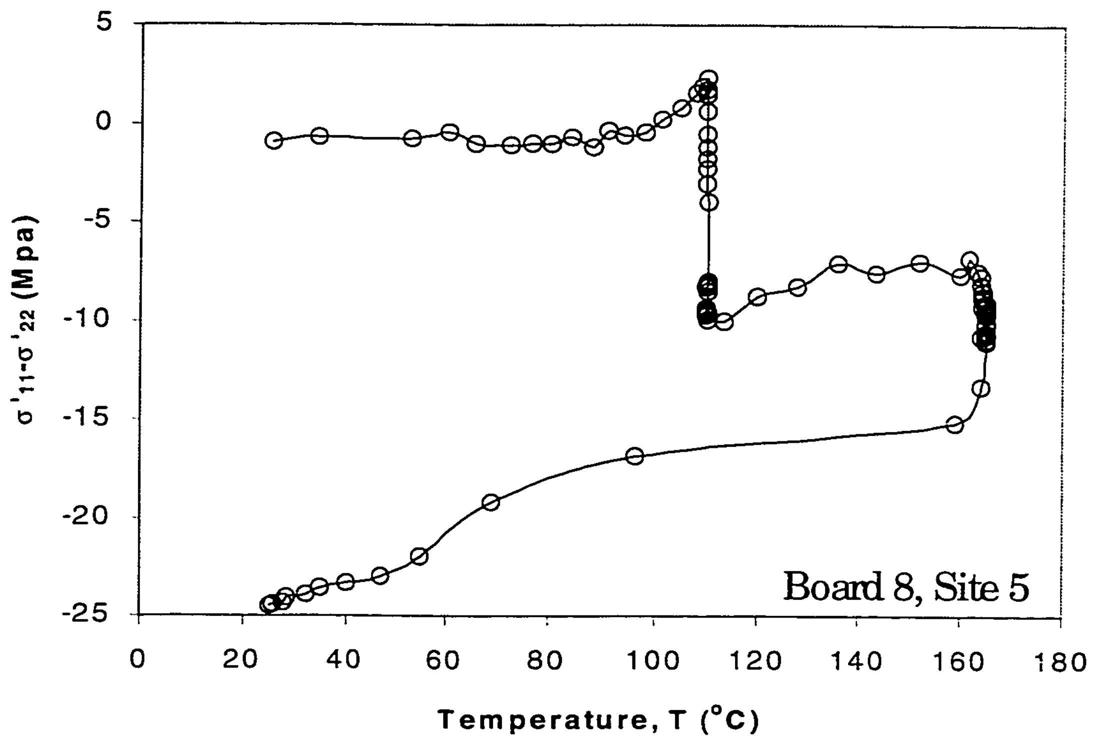

Figure 8.6 - Stress Variation During Convection Cure ($\sigma'_{11} - \sigma'_{22}$)
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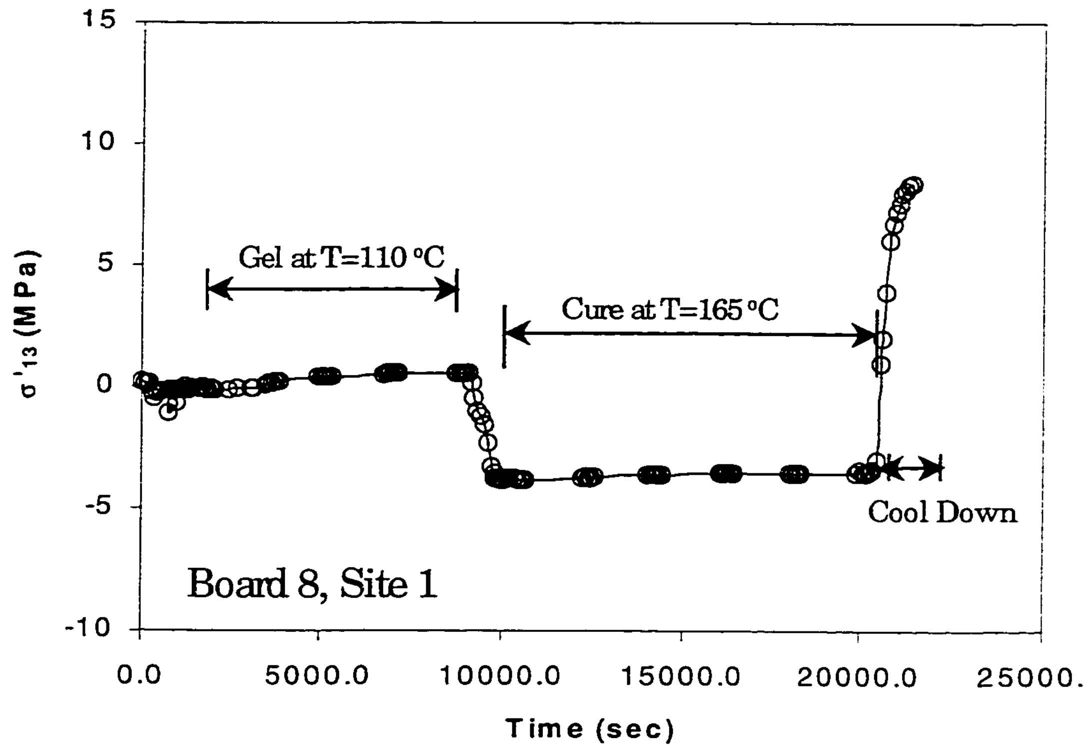

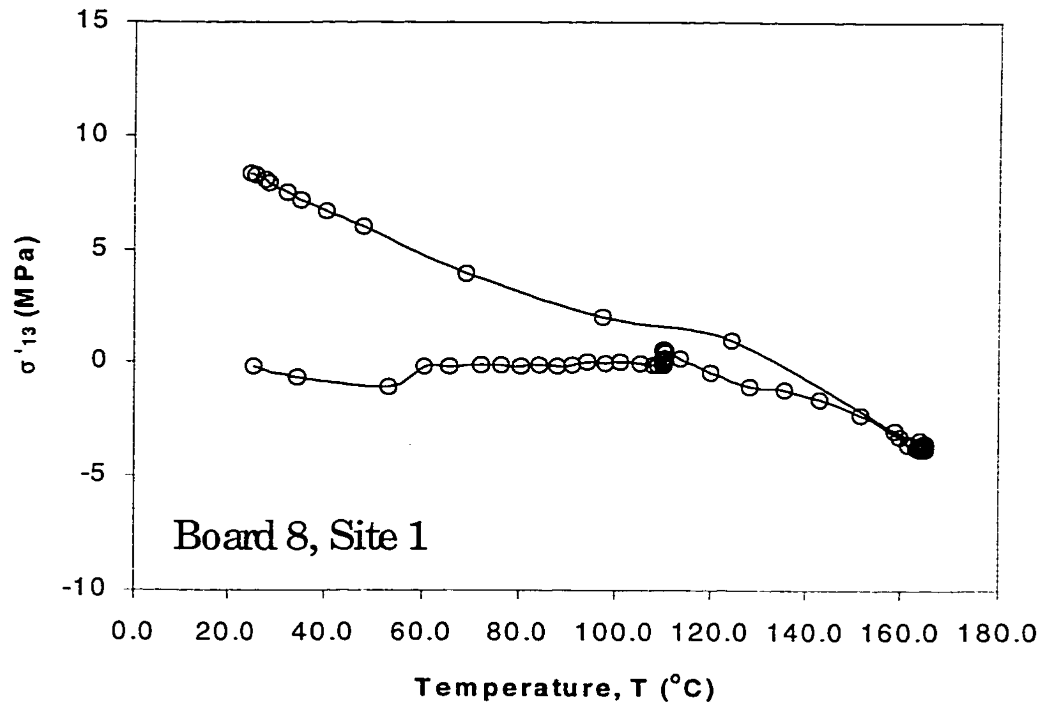

Figure 8.7 - Stress Variation During Convection Cure (σ'_{13})
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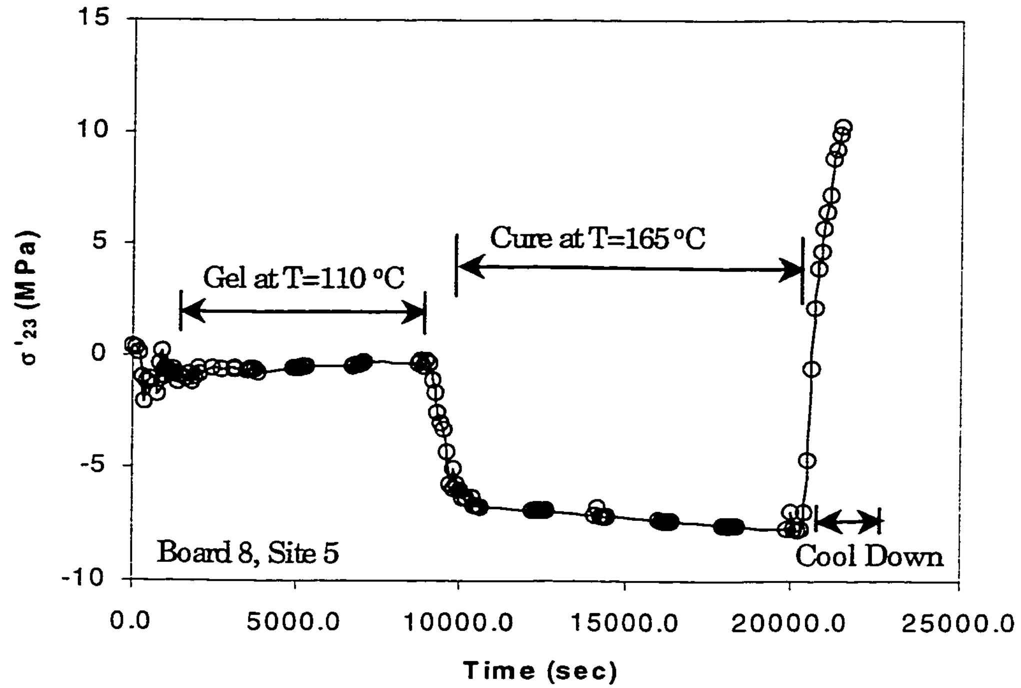

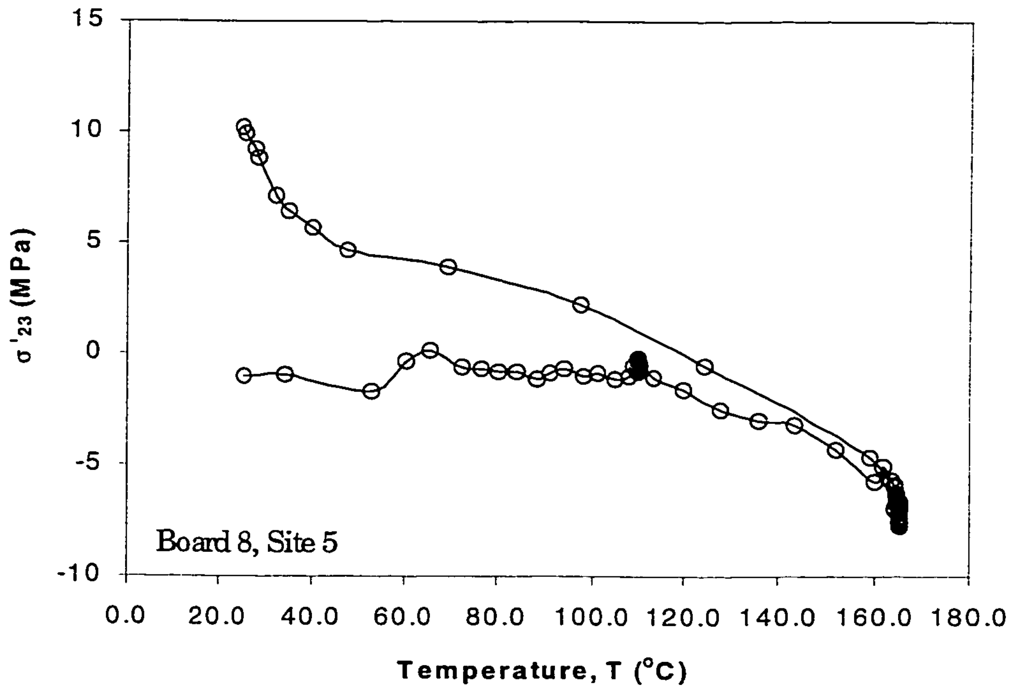

Figure 8.8 - Stress Variation During Convection Cure (σ'_{23})
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S5 in Figure 8.2). In Figure 8.7, the variation of the out-of-plane shear stress (σ'_{13}) with time and temperature is shown for site 1 (location S1 in Figure 8.2). All the data shown in Figures 8.5-8.8 are from one of the encapsulated test die (Board #8). The sites chosen for demonstration of the stress variation with time and temperature during encapsulant curing were those where relatively large stress magnitudes were found. At time t = 0, the board had just been removed off of the hot plate after dispensing of the encapsulant, and inserted into the edge connector socket to initiate data collection. The sample was inserted into the convection oven at approximately t = 400 sec for the gel portion of the encapsulant cure cycle. Between t = 400 sec and t = 2000 sec, the sample increased in temperature and eventually reached the gel temperature of 110 °C. The sample then remained at this temperature for 2 hours. At approximately t = 10000, the oven temperature was increased to 165 °C for the second portion of the encapsulant cure cycle. Upon completion of the 3 hours hold at 165 °C, the board was removed from the oven and allowed to cool in a room temperature environment.

As seen in Figures 8.5-8.8, the majority of the final stresses in the die were developed during the cool down period, where the encapsulant is fully hardened and can provide a significant stiffness to stress the low CTE silicon die material. A more complete discussion of the die stress variation during the convection cure cycle has been given in Chapter 7.

In addition to the conclusions made in Chapter 7, several further observations are presented here. The duration of the encapsulant curing cycle was 5 hours in the current study, and 2 hours in the investigation reported in Chapter 7. The longer curing time is

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recommended to minimize assembly warpage. Also, significant variations were observed in the normal stress difference during the longer gel and cure cycles, suggesting that the duration of the encapsulant shrinkage could be continued for longer times. Changes in the curing procedures for a given encapsulant could cause significant material property changes, leading to various end results including low warpages after the encapsulation process. In finite element simulations, a "stress free" state for the whole package system is usually assumed at the glass transition temperature of the encapsulant to simplify the modeling. Figures 8.5-8.8 indicate that this assumption is not true, and that more sophisticated models are needed to capture all phenomena that lead to the final stress state in electronic packages such as the COB assemblies investigated here.

Typical variation in the out-of-plane shear stresses with time and temperature during encapsulant curing process are presented in Figures 8.7-8.8. The unique capabilities of (111) silicon stress sensors to measure such stresses could also serve to reveal interfacial delaminations between the silicon die and encapsulant. Finally, lower precision should be expected in the portions of the curves in Figures 8.5-8.8 where fast temperature changes were occurring. This is due to the speed of the data acquisition system.

8.5 Stresses After Encapsulation

The final stresses resulting from the encapsulant cure cycle and COB package cooling were calculated from the original (wafer level) and final (packaged) die sensor resistances, and Eqs. (4.4, 4.5). Since both of these measurements and the calibration of the piezoresistive coefficients were done at room temperature (23 °C), any unexpected

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thermal errors will be minimized. Figure 8.9 contains the measured data for the in-plane shear stress σ'_{12}, the in-plane normal stress difference (σ'_{11} - σ'_{22}), and the out-of-plane shear stresses σ'_{13} and σ'_{23}, respectively. At every rosette site in each plot, results are given for both the convection cure and VFM cure processes. Each indicated value is the average of data taken from the 12 specimens used for each cure process.

No significant differences in the die stresses caused by convection and variable frequency microwave curing were observed. This is especially true for the out-of-plane shear stresses. For the in-plane shear stress, the stress magnitudes measured for convection cured specimens were slightly higher than those for VFM cured specimens (maximum stresses differed by 25%). However, the opposite trend was observed for the in-plane normal stress difference (maximum stresses differed by 14%). The out-of-plane shear stress magnitudes are relatively small for both curing processes when compared to the magnitudes of the in-plane stress components.

To further illustrate the nature of the stresses induced by encapsulation, two COB specimens (one from each type of cure process) were subjected to a slow temperature change from –40 °C to +125 °C. Resistance values were monitored continuously, and the stresses were extracted as a function of temperature. When using Eqs. (4.4, 4.5), it was assumed that the piezoresistive coefficients were approximately independent of temperature. Typical in-plane shear stress, in-plane normal stress difference, and out-of-plane shear stress data are shown in Figures 8.10-8.13. In all cases, raising the temperature from room temperature decreases the magnitude of the stress component. As

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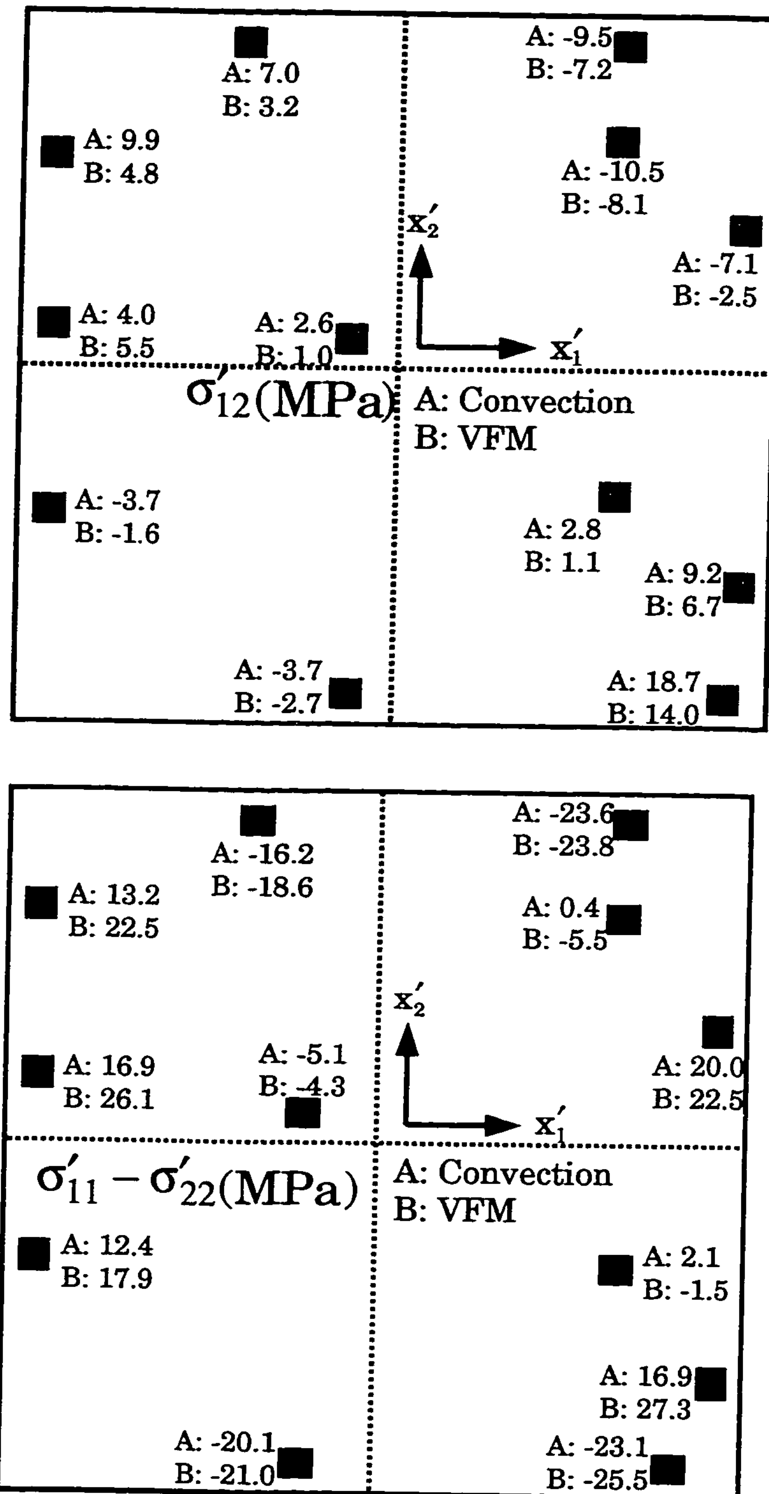

Figure 8.9 - Die Stresses after Encapsulation (COB Study #2)

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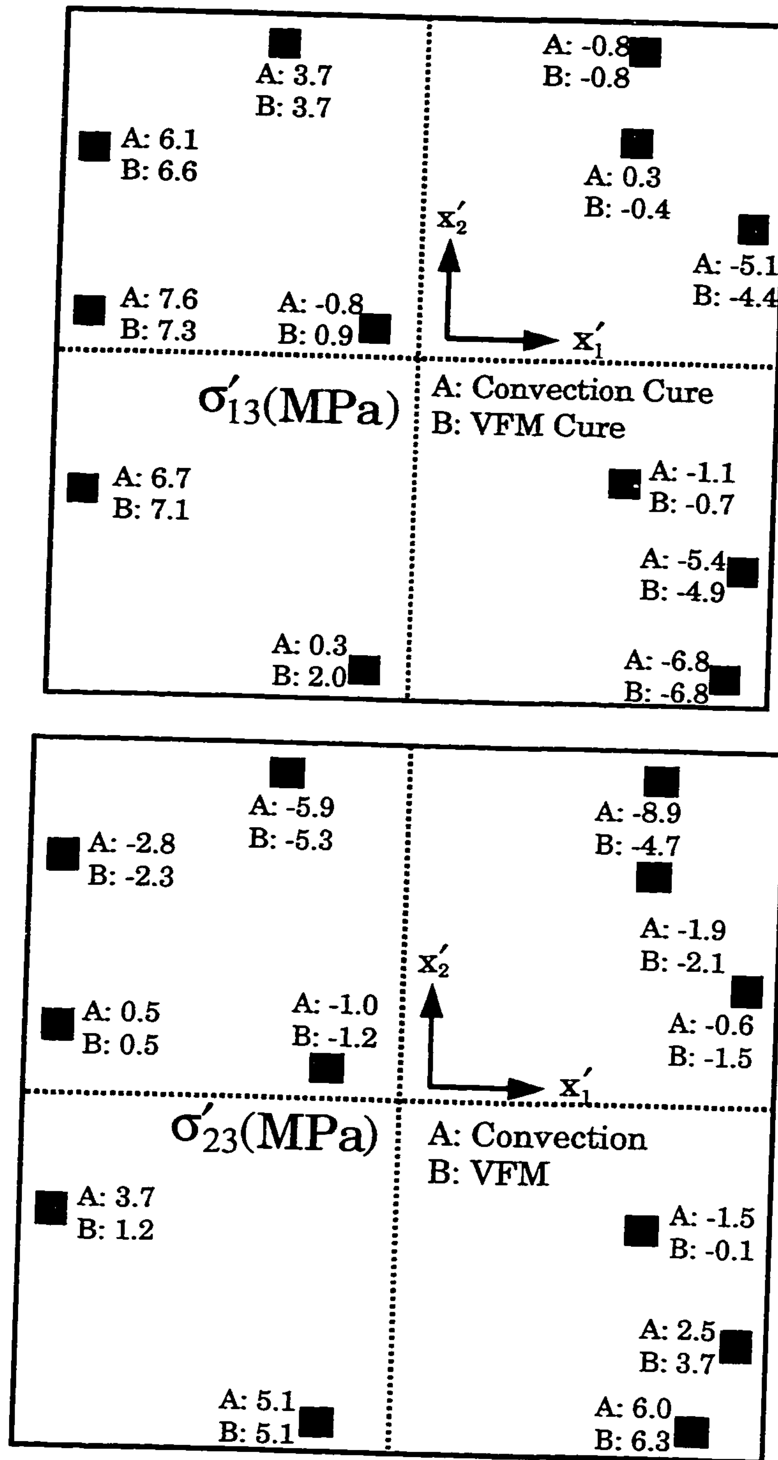

Figure 8.9 - Die Stresses after Encapsulation (COB Study #2)
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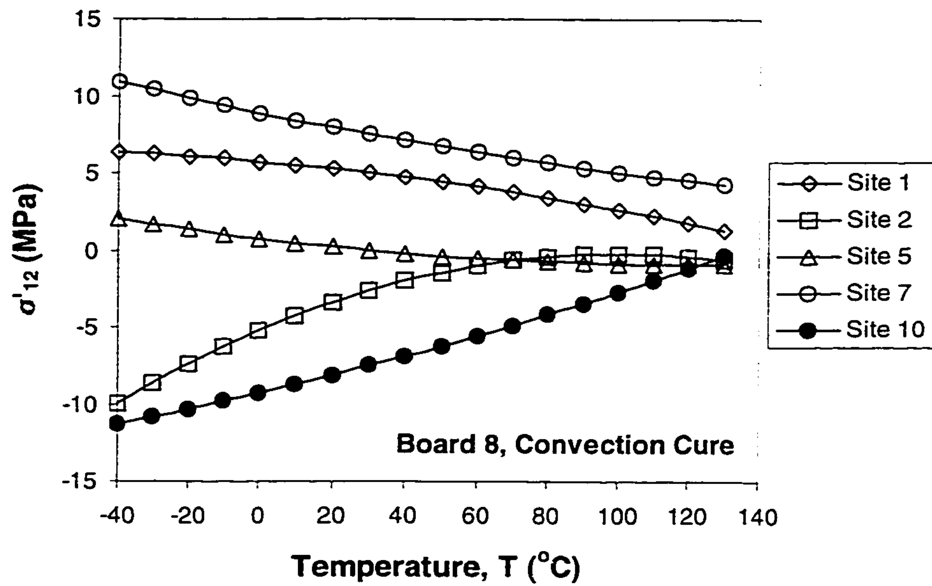

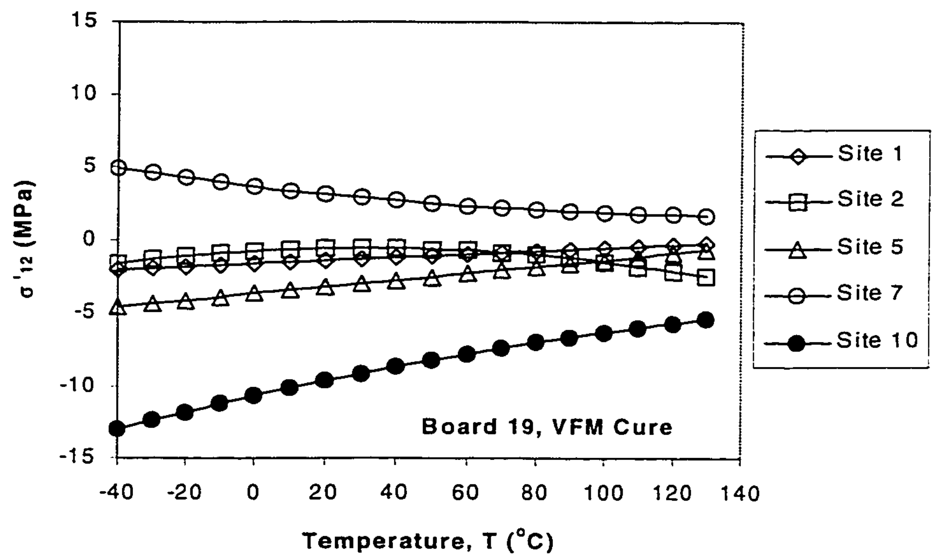

Figure 8.10 - Variation of Final Packaged Die Stress with Temperature (σ'_{12}) (COB Study #2)

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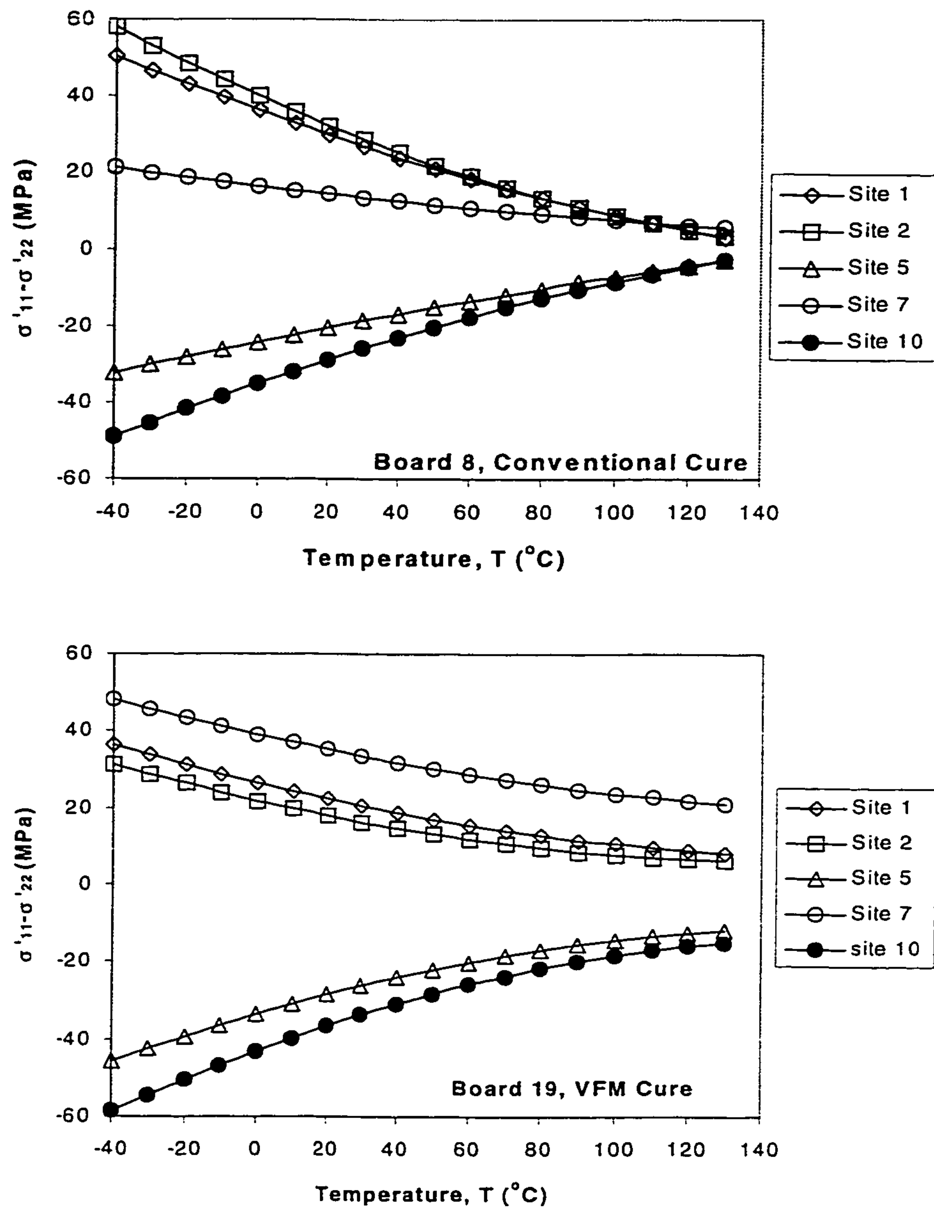

Figure 8.11 - Variation of Final Packaged Die Stress with Temperature ($\sigma'_{11} - \sigma'_{22}$) (COB Study #2)

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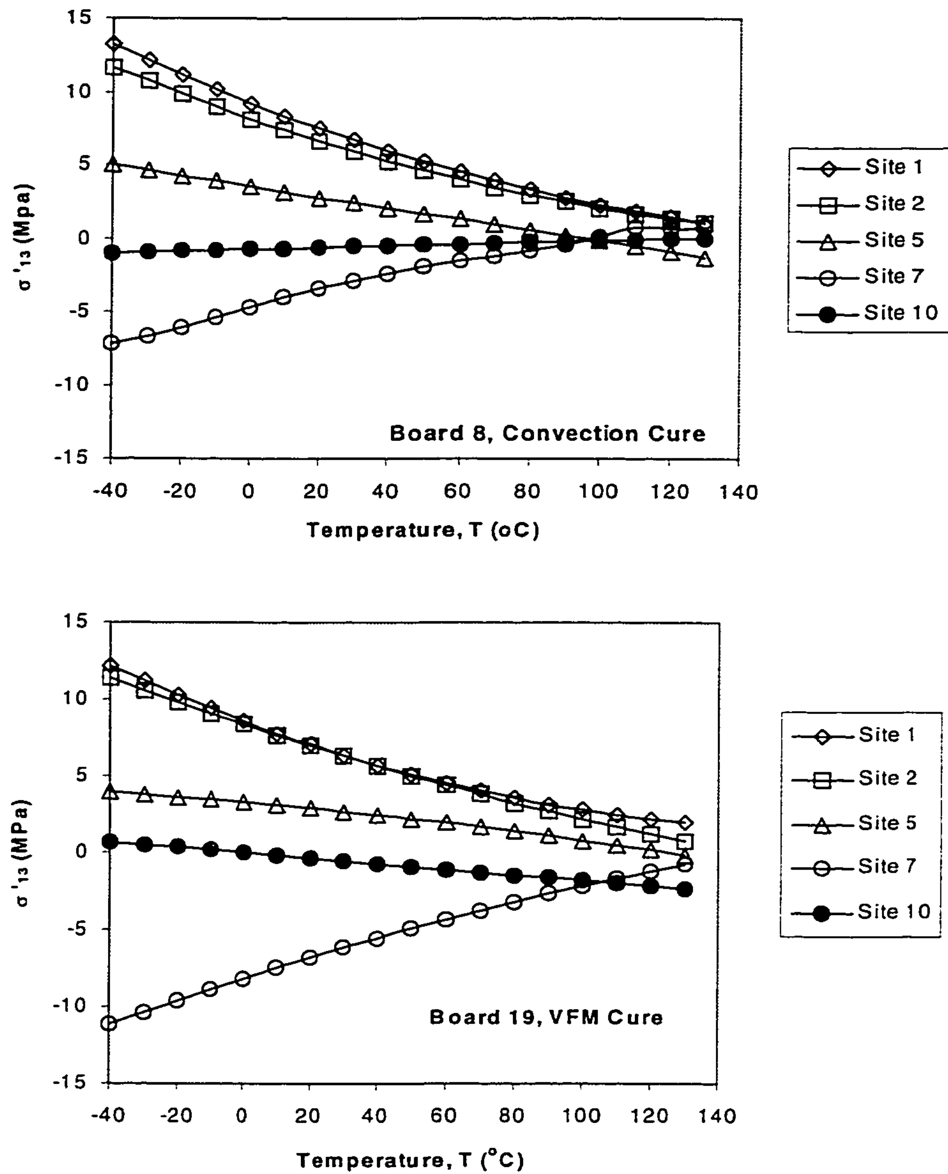

Figure 8.12 - Variation of Final Packaged Die Stress with Temperature (σ'_{13}) (COB Study #2)

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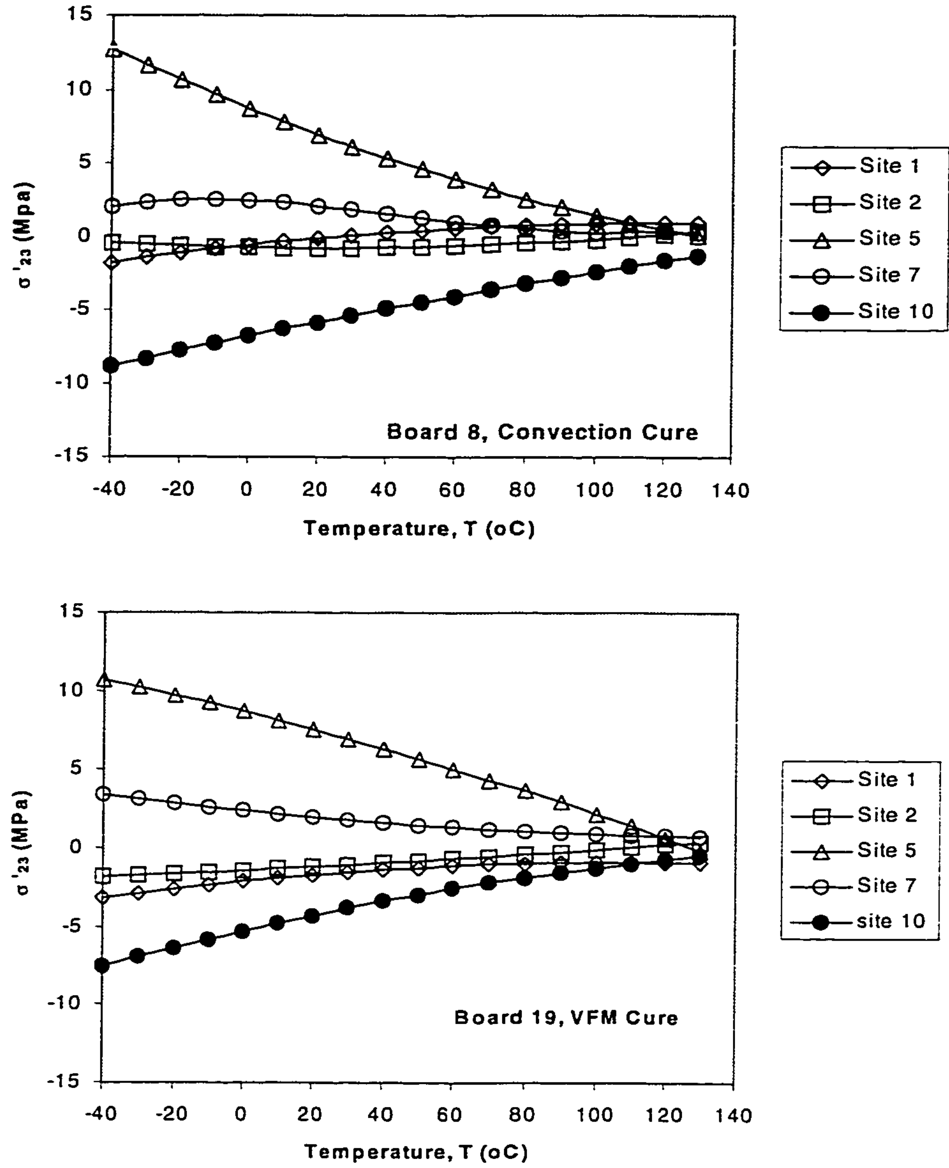

Figure 8.13 - Variation of Final Packaged Die Stress with Temperature (σ'_{23})
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the temperature approaches 165 °C (the final cure temperature of the liquid encapsulant in both processes), the stresses approach zero. Likewise, at lower temperatures the stress levels are increased. This is because the material expansion mismatch becomes worse due to the larger temperature change from the “relaxed” configuration of the package materials at approximately 165 °C.

Similar trends were found in the stress variations with temperature for both the convection and VFM curing processes. As discussed above, the glass transition temperature and the curing temperature of the encapsulant are most probably not the "stress free" temperature for the whole package system. However, it is still valuable to assume a "stress free" state at the glass transition temperature of the encapsulant to simplify the FEM modeling. One factor causing nonlinearities in the stress versus temperature curves is likely the temperature dependent material properties of the encapsulant. Table 8.1 shows the temperature dependent values of the coefficient of thermal expansion and elastic modulus of Hysol FP4651. Large CTE changes occur between 120 °C and 190 °C, which might cause nonlinearity in the stress versus temperature curves.

E (GPa)	14.3 (-40 °C)	13.7 (25 °C)	11.0 (125 °C)
α (ppm/°C)	11-13 (40-120 °C)	50 (190-220 °C)	

Table 8.1 - Temperature Dependent Material Properties of Hysol FP4651

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8.6 Finite Element Simulations

The final room temperature experimental results have been evaluated through correlation with the predictions of nonlinear three-dimensional finite element simulations of the packaging process. In the finite element models, the materials were modeled as linear elastic. Temperature dependent mechanical properties and large deformations (kinematic nonlinearities) were utilized. The time dependent (viscoelastic) behavior of the liquid encapsulant was neglected to simplify the analysis, and because of a lack of material characterization data. A full model of the specimen was meshed. Figure 8.14 depicts the COB encapsulation sample dimensions used in the FEM simulations. The temperature dependent material properties of Hysol FP4651 were listed in Table 8.1. The mechanical properties of the other materials in the COB package were listed in section 7.3. The die was assumed to be stress free at the glass transition temperature of the filled epoxy encapsulant (150 °C), and cooling from the glass transition temperature to room temperature was simulated. In general, the curing procedures for the encapsulant are complex, even for the convection oven cure approach. The curing processes affect the encapsulant material properties significantly as explained in Chapter 7. Therefore, the modeling approach used provides only an introductory understanding of the stress development in the COB assemblies. The variable frequency microwave curing consists of even a more complex procedure (Figure 8.3), which is almost impossible to simulate by means of finite element methods.

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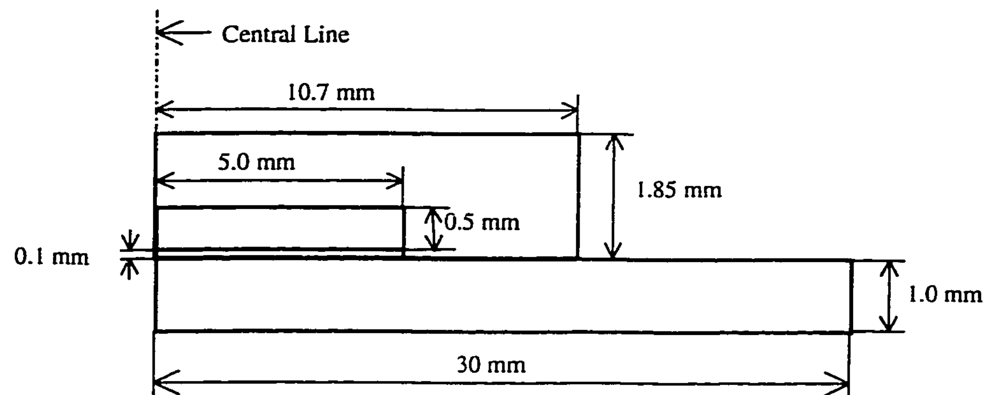

Figure 8.14 - Dimensions of COB Encapsulation Model

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Figure 8.15 illustrates temperature compensated experimental measurements and finite element predictions for the die surface distributions of the in-plane shear stress σ'_{12}, in-plane normal stress difference (σ'_{11} - σ'_{22}), and the out-of-plane shear stresses σ'_{13} and σ'_{23}, respectively. In these plots, the colored contours are the room temperature stress distributions predicted by the finite element model. Each of the small squares in these diagrams locates a sensor rosette site. The color of a given square represents the average room temperature experimental value of the stress at the rosette site, when considering the results for all 12 specimens (the square is colored to the same scale/legend of the finite element contours). These experimental data are the same as shown in Fig. 8.6 for the convection curing.

It can be see that the finite element predictions are in reasonable agreement with the experimental results. The measured stresses show the same trends and numerical signs as the distributions predicted by finite element analysis. The correlations of the experimental and numerical shear stress values are excellent. However, the finite element model over predicts the observed normal stress difference data since the viscoelastic relaxation of the filled epoxy encapsulant was neglected.

8.7 Stresses Due to Thermal Cycling and Moisture Absorption

After performing the measurements discussed above, the samples from each curing method were divided into two groups, and reliability tests were carried out to evaluate the capability of the COB samples to survive a variety of severe environments. Specimens from the first group were subjected to thermal cycling between –40 °C and

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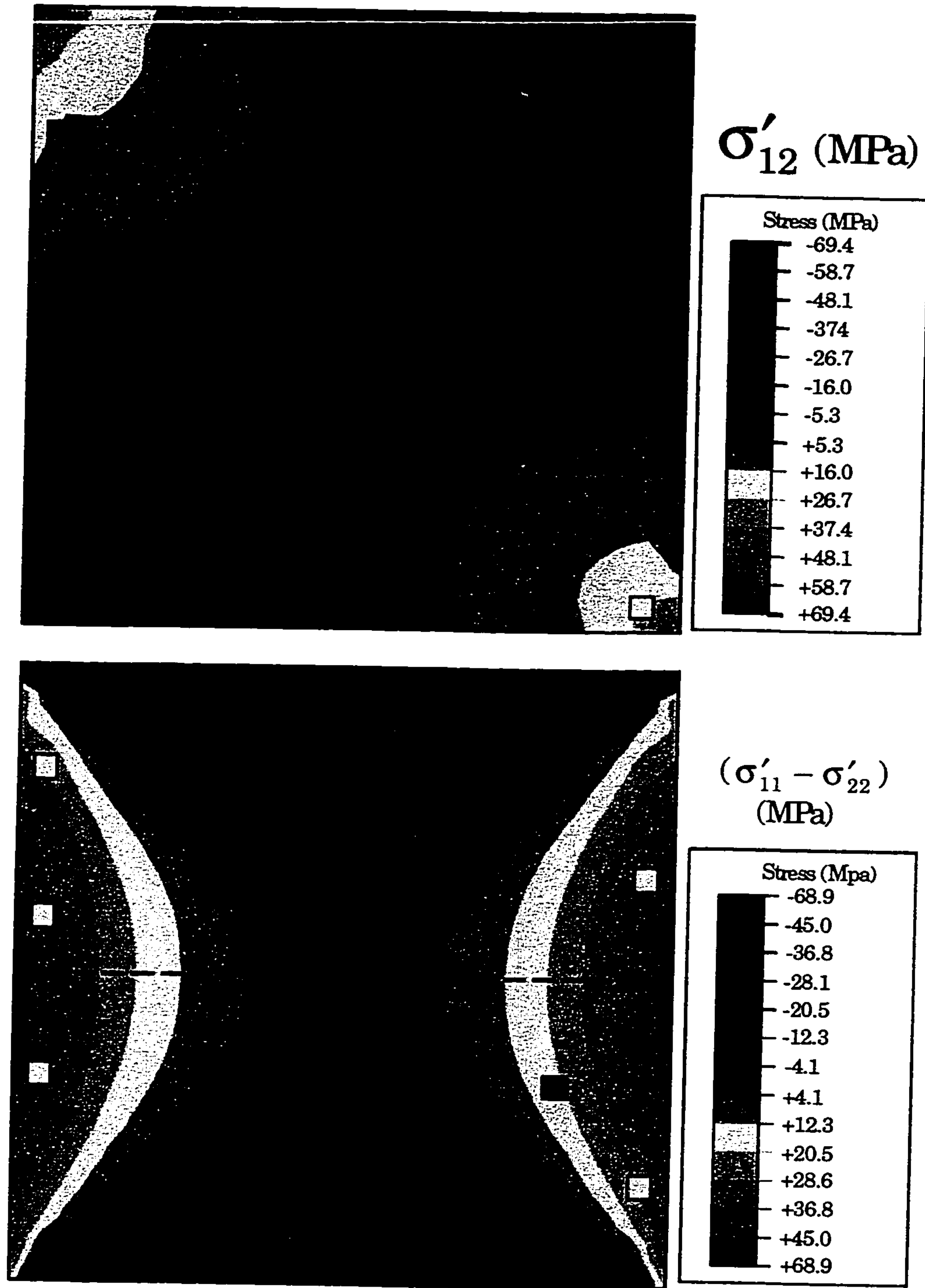

Figure 8.15 - Finite Element Contours and Experimental Data
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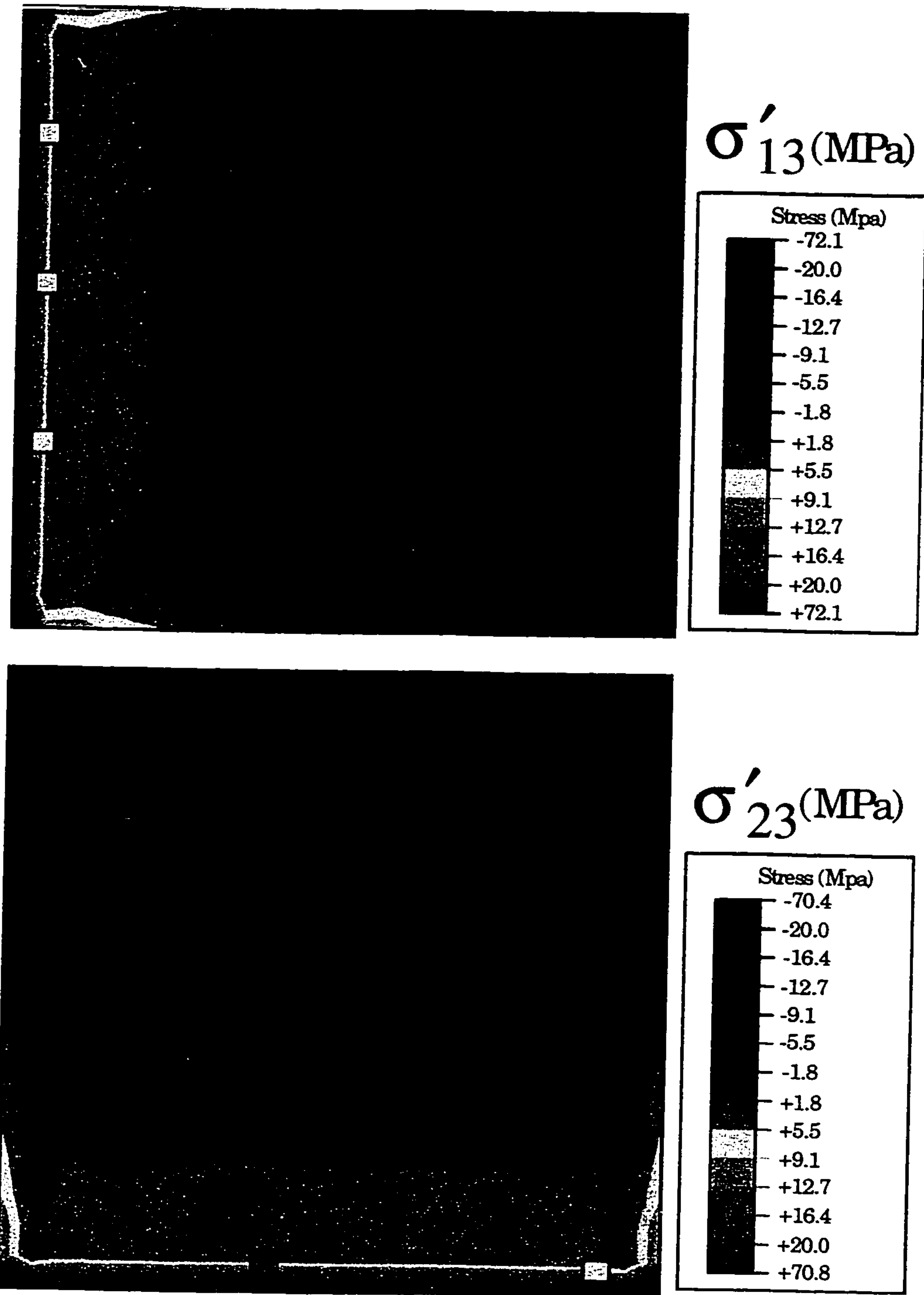

Figure 8.15 - Finite Element Contours and Experimental Data
(COB Study #2)

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+125 °C. A total of 2000 thermal cycles were completed. The second group was exposed to high humidity storage at 85% RH and 85 °C for 168 hours. In each case, changes in the die stress levels were monitored for samples from each curing method in order to detect delaminations and other failures, and to study the impact of moisture absorption. A brief discussion of the observed results is now presented.

The thermal cycling tests have been performed in five stages (100, 100, 700, 600, and 500 cycles) for a total of 2000 cycles. After each round of cycling, the samples were taken out of the oven and the resistances of all the sensors on the test die were recorded at room temperature. The die stresses after each thermal cycling iteration were then extracted by using Eqs. (4.4, 4.5). Figures 8.16-8.19 illustrate the stress variations during the thermal cycling tests for the in-plane shear stress (σ'_{12}), in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$), and out-of-plane shear stress (σ'_{13} and σ'_{23}), respectively. The stress changes at various points in the cycling show similar trends for the two curing processes. Small stress increases were observed in the in-plane normal stress difference (σ'_{11} - σ'_{22}), demonstrating that further curing of the encapsulant could be occurring during the early thermal cycling. Conversely, a small amount of stress decrease/relief is illustrated in the in-plane shear stress (σ'_{12}) data for both cure methods. This indicates potential creep of the epoxy material and/or possible initiation of delaminations or encapsulant cracking. With very few exceptions, the stress variations for all the temperature compensated stress components were small over the 2000 cycles for both curing methods. Delaminations were detected at five rosette sites in the convection cured parts. Data from these sites were neglected in the averages shown in Figures 8.16-8.19.

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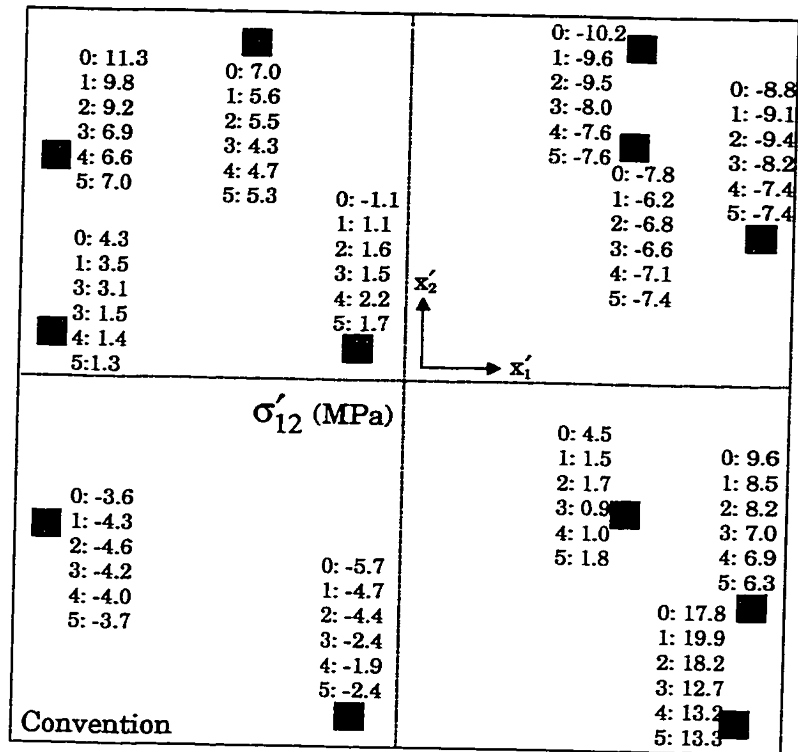

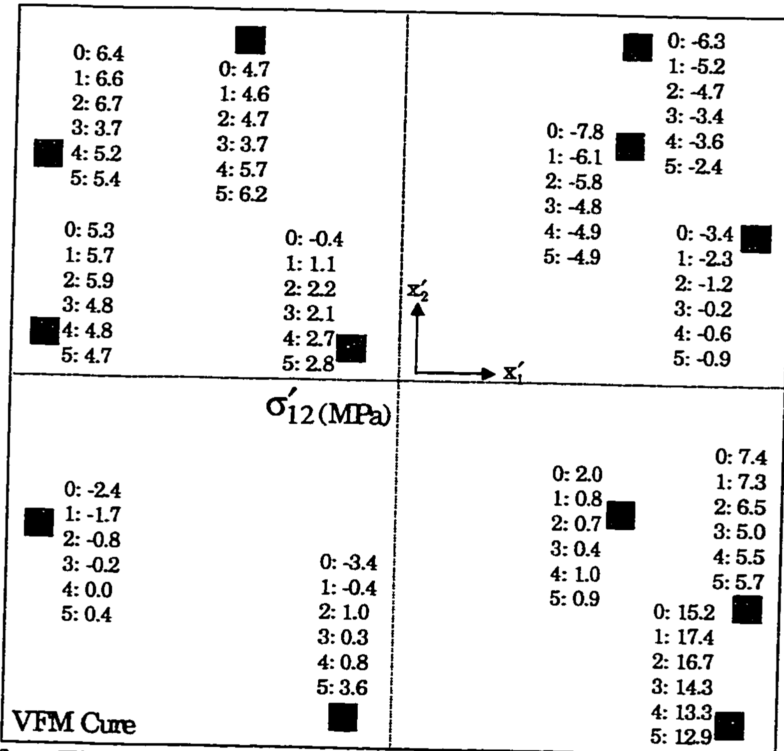

(0: Before Thermal Cycling, 1: After 100 Cycles, 2: After 200 Cycles, 3: After 900 Cycles, 4: After 1500 Cycles, 5: After 2000 Cycles)

Figure 8.16 - Stress Variations Due to Thermal Cycling (σ'_{12}, COB Study #2)

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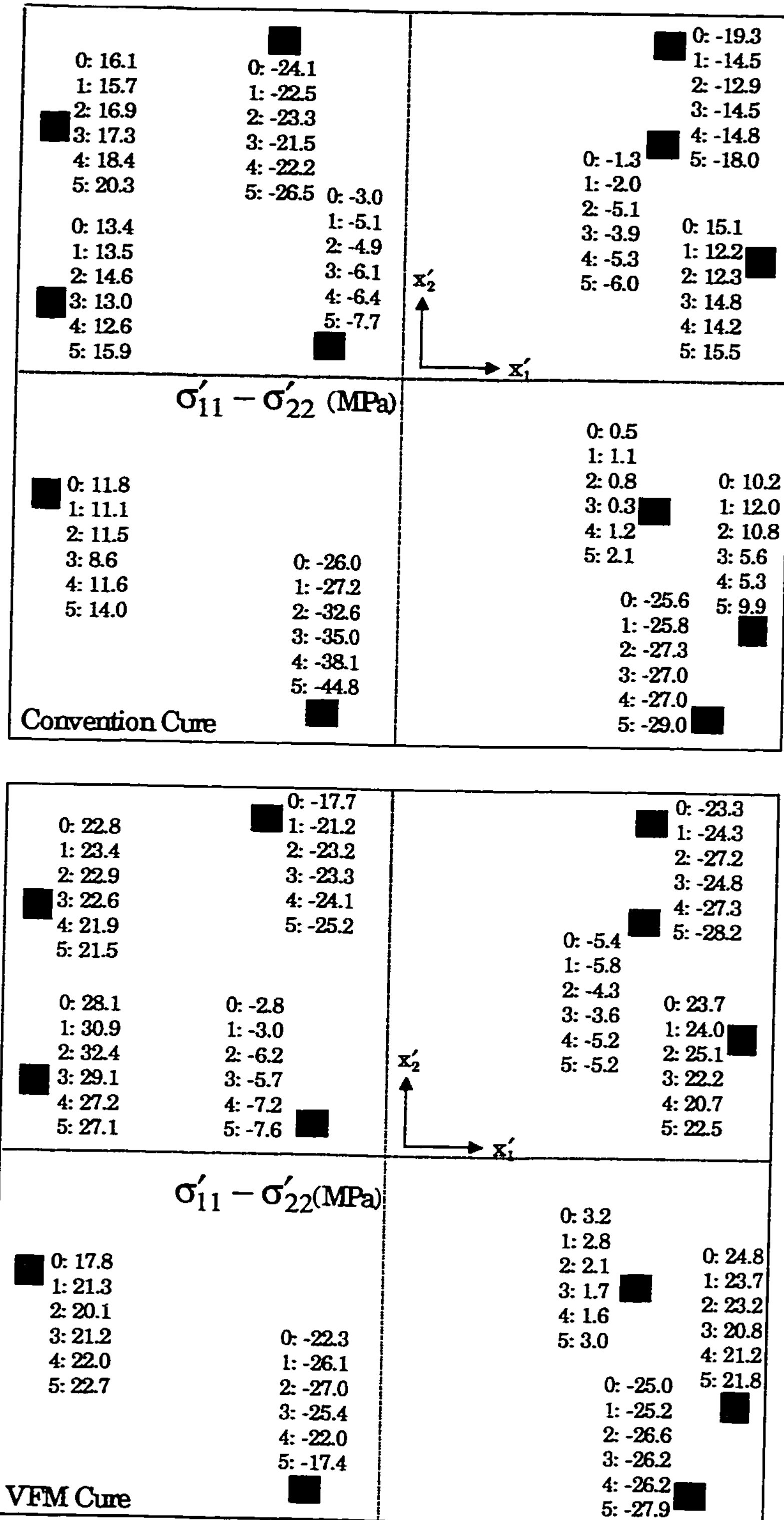

(0: Before Thermal Cycling, 1: After 100 Cycles, 2: After 200 Cycles, 3: After 900 Cycles, 4: After 1500 Cycles, 5: After 2000 Cycles)

Figure 8.17 - Stress Variations Due to Thermal Cycling ($\sigma'_{11} - \sigma'_{22}$, COB Study #2)

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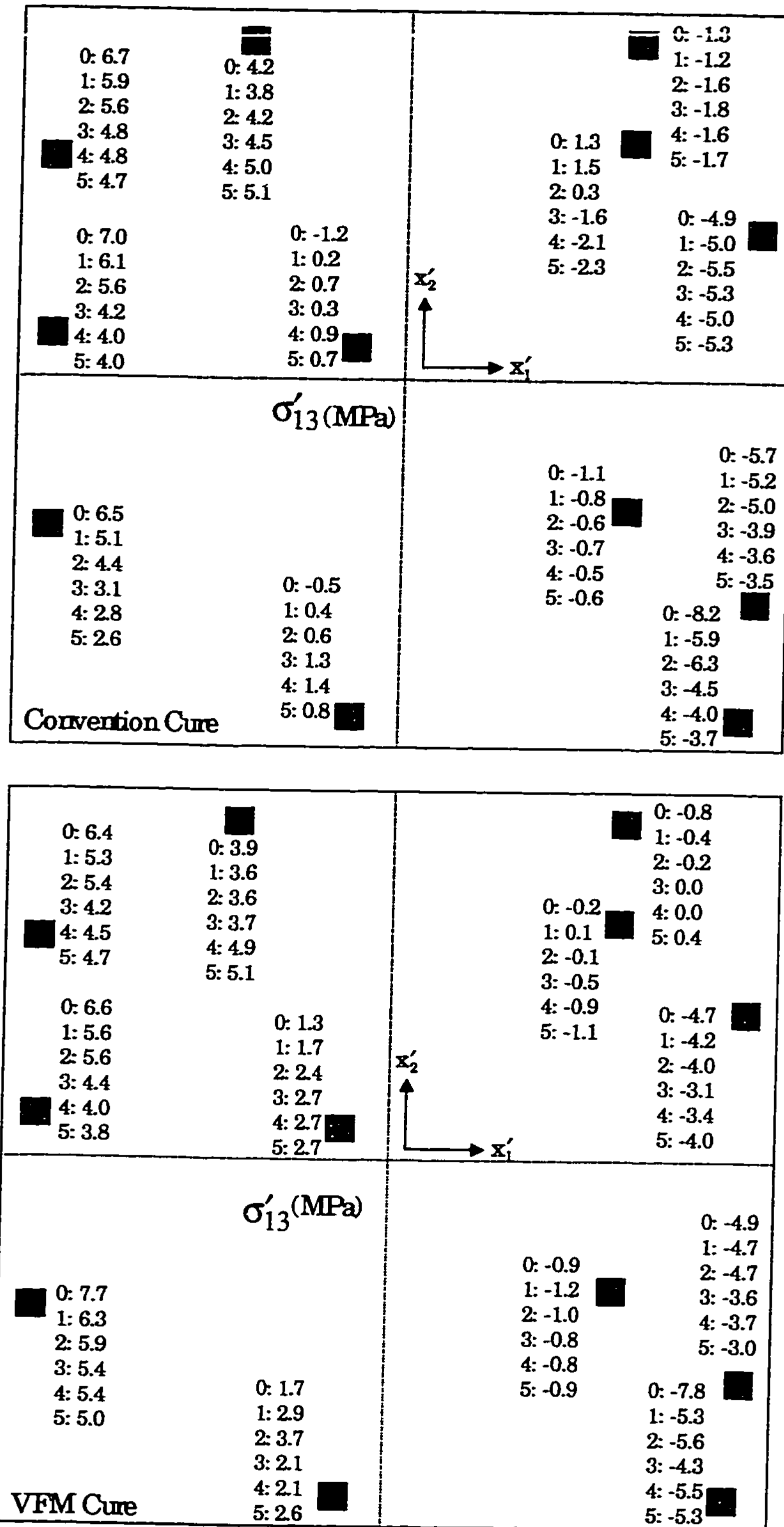

(0: Before Thermal Cycling, 1: After 100 Cycles, 2: After 200 Cycles, 3: After 900 Cycles, 4: After 1500 Cycles, 5: After 2000 Cycles)

Figure 8.18 - Stress Variations Due to Thermal Cycling (σ'_{13}, COB Study #2)

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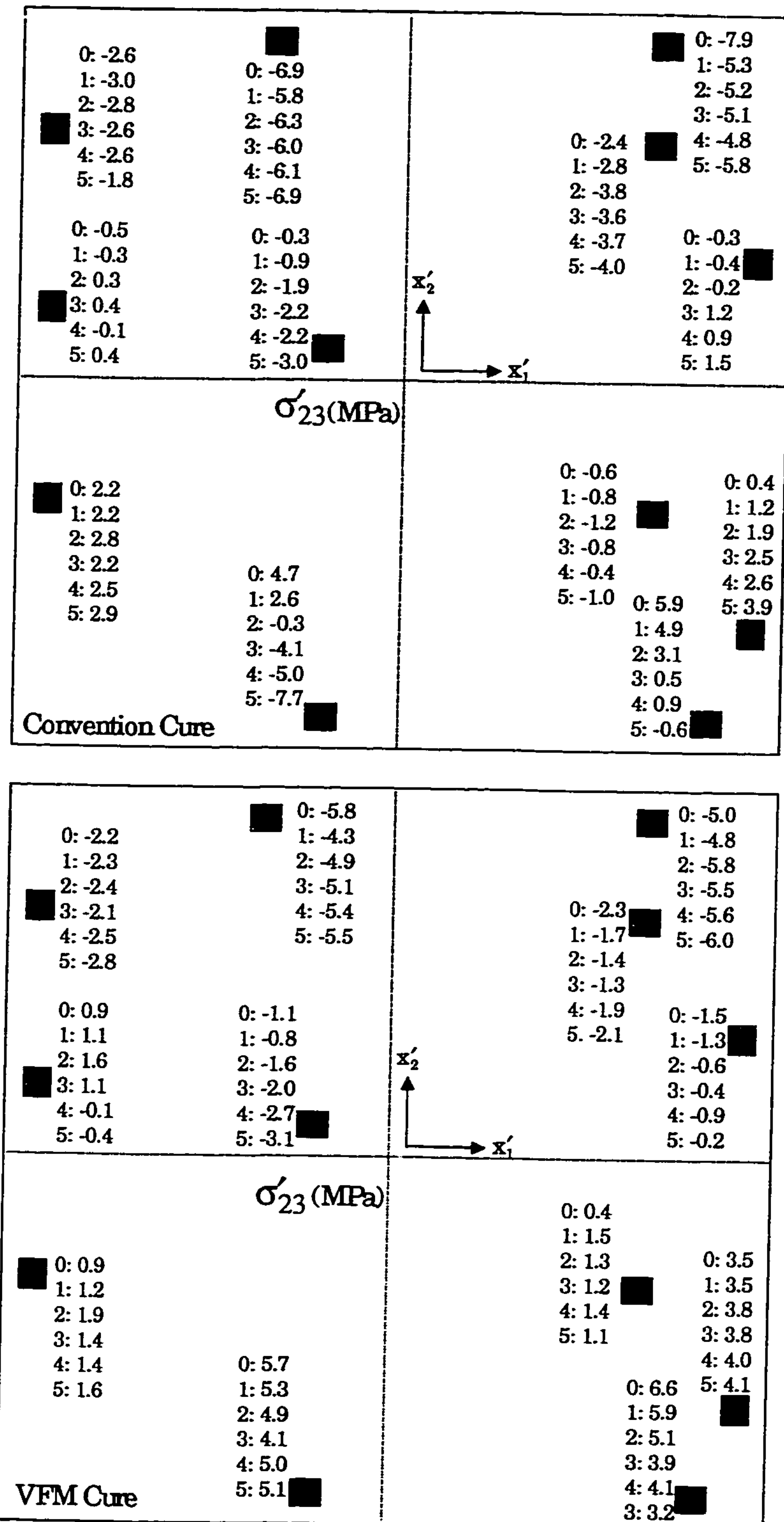

(0: Before Thermal Cycling, 1: After 100 Cycles, 2: After 200 Cycles,
3: After 900 Cycles, 4: After 1500 Cycles, 5: After 2000 Cycles)

Figure 8.19 - Stress Variation Due to Thermal Cycling (σ'_{23}, COB Study #2)

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No failures were detected in the VFM cured samples. These results illustrate similar trends for the stress variations in the samples cured with convection and VFM systems.

Room temperature stress results before and after high humidity storage (for 168 hours at 85% RH and 85 °C) are shown in Figures 8.20-8.23. The trends shown in the stress variations were found to be the same as in the thermal cycling tests, and both curing methods yielded reliable samples with no failure detected.

8.8 Summary

Die surface stresses in COB packages were measured for a commercial encapsulant cured with both convection and variable frequency microwave curing. The utilized stress test chips contained an array of optimized sensor rosettes that are capable of evaluating the complete stress at points on the surface of the die. Stresses were monitored in-situ during the convection cure cycle. However, microwave interference with the measurement signals did not permit in-situ monitoring for the VFM cure. A comparison was made between the room temperature stresses found with each method of curing. Differences from 0-25% were observed in the maximum values of the in-plane die stresses caused by convection and VFM microwave curing. Differences in the out-of-plane shear stresses produced with each cure process were minimal.

After cure, the samples from each curing method were divided into two groups, and reliability tests were performed. The first group of samples was subjected to thermal cycling over the range of –40 °C and +125 °C. The second group was exposed to high humidity storage at 85% RH and 85 °C. In both cases, the stress variations were found to

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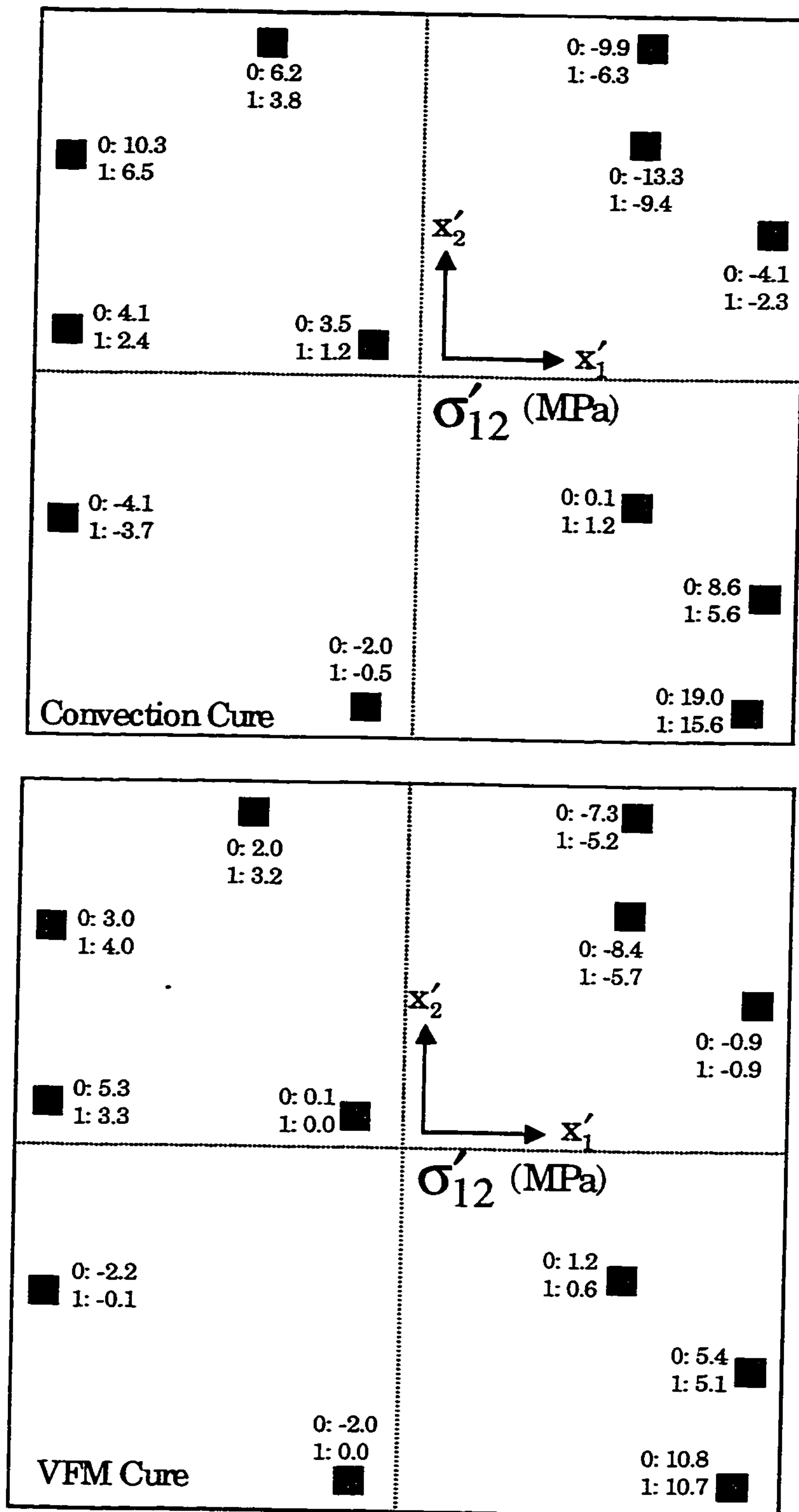

(0:Before Exposure, 1: After Exposure)

Figure 8.20 - Stress Variation Due to High Humidity Storage (σ'_{12}, COB Study #2)

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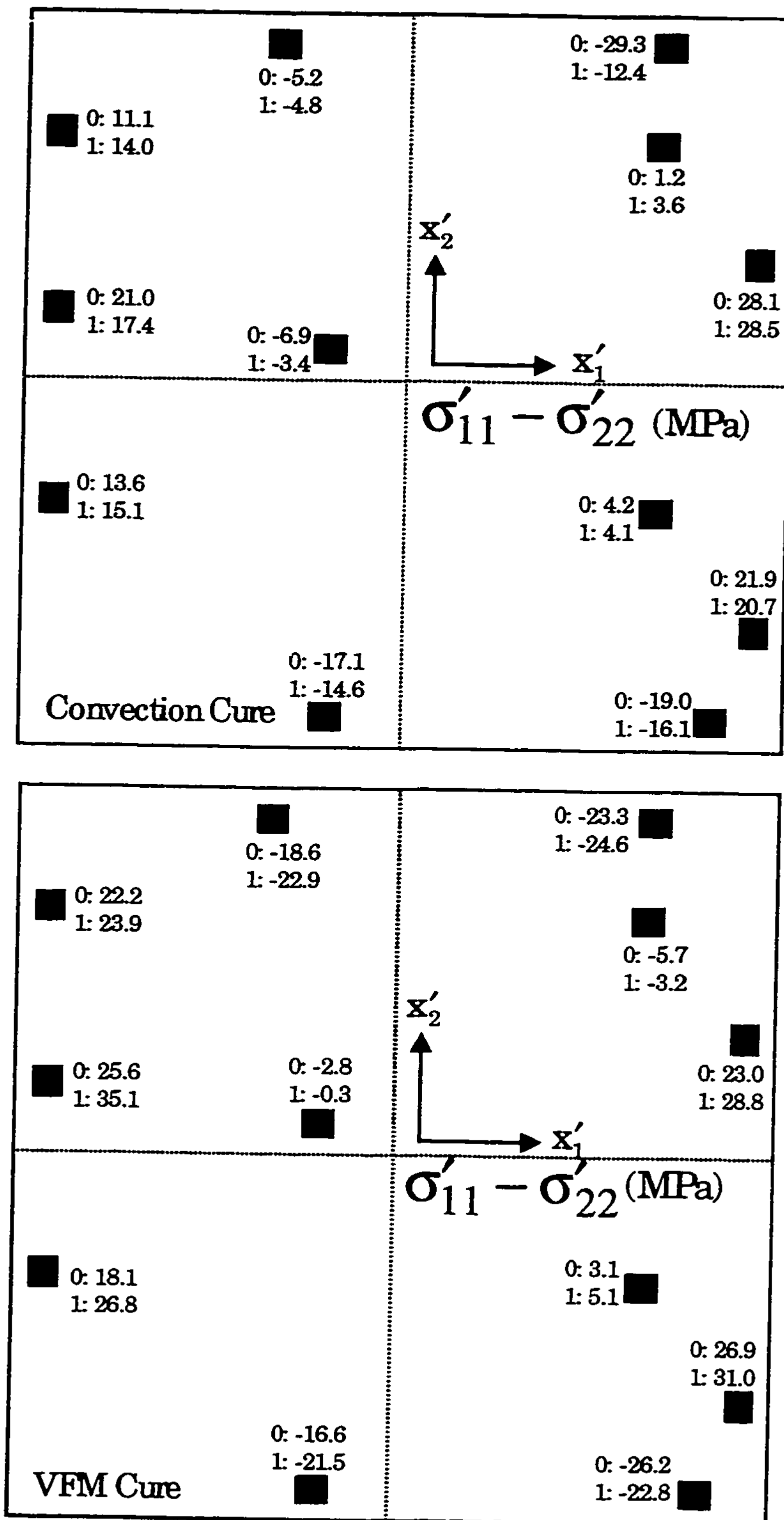

(0:Before Exposure, 1: After Exposure)

Figure 8.21 - Stress Variation Due to High Humidity Storage ($\sigma'_{11} - \sigma'_{22}$, COB Study #2)

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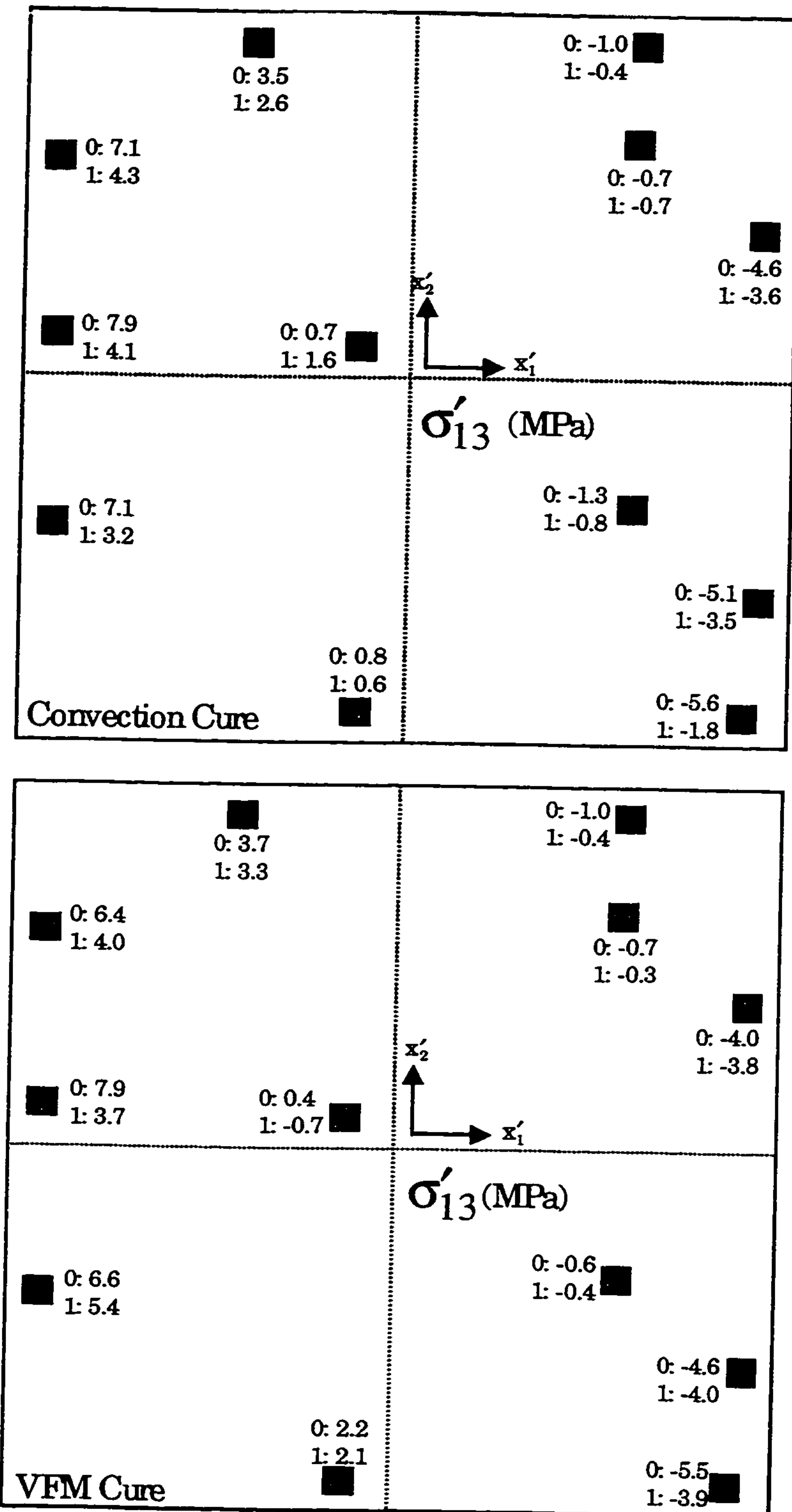

(0:Before Exposure, 1: After Exposure)

Figure 8.22 - Stress Variation Due to High Humidity Storage (σ_{13}', COB Study #2)

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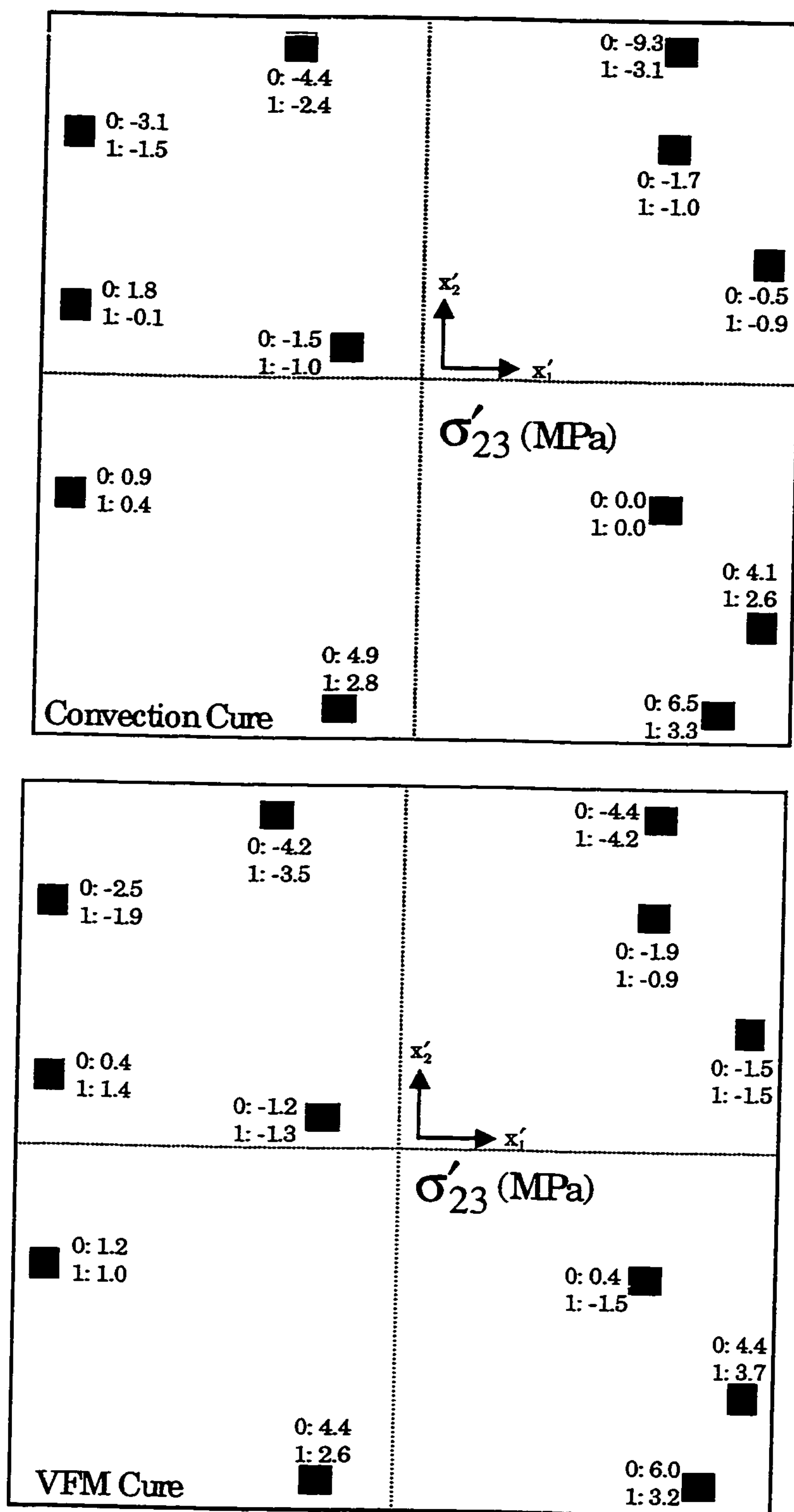

(0:Before Exposure, 1: After Exposure)

Figure 8.23 - Stress Variation Due to High Humidity Storage (σ_{23}', COB Study #2)

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be small over the entire duration of the reliability testing. However, delaminations were detected at five sites in the convection cured thermal cycling samples. Also, the results illustrated similar trends for the stress variations in the samples cured with convection and VFM systems.

Three-dimensional nonlinear finite element simulations of the chip on board packages were also performed, and the stress predictions were correlated with the room temperature experimental test chip data. The experimental shear stress results were in good agreement with the finite element predictions. However, improvement in the constitutive model for the filled epoxy encapsulant will further improve the finite element predictions of the normal stress distributions.

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CHAPTER 9

DIE STRESS MEASUREMENTS IN 281 PIN CPGA PACKAGES USING HIGH TEMPERATURE DIE ATTACHMENT MATERIALS

9.1 Introduction

Mechanical stresses produced during the die attachment assembly of microelectronic packages can cause component failure through various mechanisms such as microcracks, voids, and other defects in the die and/or die attachment materials. These stresses are often thermally induced during manufacture, test, storage, and operation. They can be significantly affected by the choice of die-attachment adhesive. To achieve reliable high temperature electronic packaging, the selection of die attachment material becomes critical.

Previous investigators have used test chips to experimentally explore the die stresses induced during die-attachment [23, 32, 117, 137-139]. Two-dimensional in-plane stresses were measured by van Kessel, et al. [32] using (111) silicon test chips with diffused resistor strain gages. They considered several die-attachment and leadframe combinations including Au-Si and Alloy 42, epoxy adhesive and copper, and polyimide adhesive and copper. Yagi and co-workers [138] used a high temperature diffused-type strain gage made on (110) silicon wafers to determine the thermal stresses induced during the die-attachment procedure. In that study, stress relaxation was observed after die

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attachment for chips attached to a nickel-plated copper substrate using Sn-Pb solder. Strains as a result of die bonding were also measured by Lanchberry and Shorthouse [139], using test chips fabricated on (110) silicon wafers. They considered four substrate materials: alumina, tungsten/copper alloy, molybdenum, and copper. Zou, et al. [23,117] have measured three-dimensional die attachment stresses in chip-on-board and 240 pin Quad Flat Pack (QFP) packages using (111) silicon test chips. In these studies, the magnitudes of the die attachment stresses were shown to be fairly low (under 10 MPa), and were found to be much lower than the stresses induced by encapsulation).

In this work, the variation of die stress during thermal cycling and thermal aging reliability tests has been explored experimentally using test chips. Silicon (111) stress test die containing an array of optimized piezoresistive sensor rosettes have been used to characterize die stresses within 281-pin ceramic PGA packages. Eight element dual polarity rosettes were used to evaluate the complete stress state at points on the surface of the die. Calibrated and characterized test chips were attached to the PGA packages using six high temperature die attachment adhesives designed for avionic applications. The adhesive systems included silver filled glasses, polyimide pastes, thermoplastic films, and gold germanium adhesives. The resistances of the sensors were recorded at room temperature before and after die attachment. The induced thermal stresses at sites on the die surface were then calculated using the measured resistance changes and piezoresistive theory. A comparison of the room temperature and elevated temperature die stresses caused by the different die-attachment materials has been made. After the initial stress measurements, thermal aging and thermal cycling tests were conducted on the packages,

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and the measured changes in stress were used to further differentiate the various die attachment materials. Finally, three-dimensional finite element simulations of the PGA packages were performed, and the stress predictions were correlated with the experimental test chip data.

9.2 281 Pin CPGA Package Studies

In this study, the (111) test chips were directly attached to the ceramic PGA packages using six different high temperature die attachment materials (denoted as adhesives A through F). The material type, curing conditions, cured thickness, and vendor supplied material properties for each adhesive are listed in Table 9.1. The die attachment material thicknesses were measured using the vertical micrometer of an optical microscope (200X magnification, depth of field of approximately 1.2 μm). Fine aluminum wires were used to provide the interconnections from the die bond pads to the metal traces on the PGA's. The PGA packages were then sealed using Kovar lids and an Au-Sn eutectic pre-form. Figure 9.1 shows a photograph of a typical PGA package (lid removed), and Figure 9.2 shows all the accessible rosette sites for stress measurement. A total of 20 rosette sites on the die were monitored in each package. The test chips were cut from the wafers so that the (x'_1, x'_2) wafer axes were along the horizontal and vertical edges of the test chip layout shown in Figure 9.2. The utilized (111) silicon test chips were from the BMW2.1 wafer lot, and the piezoresistive coefficient calibration results were listed in Table 4.2.

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Material	Material Type	Curing Condition	Cured Thickness (mils)	Material Properties			
				E (10^6 psi)	ν	CTE (10^{-6} 1/°C)	T_g (°C)
A	Silver-Filled Glass	12 minutes at 410 °C	4.6	3.02	.23	11	270-290
B	Silver-Filled Glass	7 minutes at 407 °C	4.7	2.19	.25	22	290
C	Polyimide	200 °C	2.7	0.7	.3	37	120
D	Polyimide	275 °C	3.1	1.3	.22	41	240
E	Thermoplastic Film	375 °C	5.6	$\geq$ 0.36	*	43	180
F	Au/Ge	385 °C	*	10	*	11	356

Notes: E = Elastic Modus, ν = Poisson's Ratio, CTE = Coefficient of Thermal Expansion, T_g = Glass Transition Temperature

Table 9.1 – High Temperature Die Attachment Materials and Properties

Before packaging, the initial room temperature resistances of all of the sensors on the test die were recorded using an automated probe station. The characterized test chips were then attached to the PGA's using the vendor recommended assembly and curing procedures, and the post packaging room temperature resistances of the sensors were recorded. At least 10 samples were fabricated for each of the die attachment materials. Two of the samples for each material were also subjected to a single thermal cycle, and transient sensor resistances were monitored continuously. Finally, thermal cycling and thermal aging qualification tests were performed on all of the packages to assess the long-term reliability of each die attachment material. The resistances of the sensors were subsequently recorded after each reliability test step. Using the measured resistance

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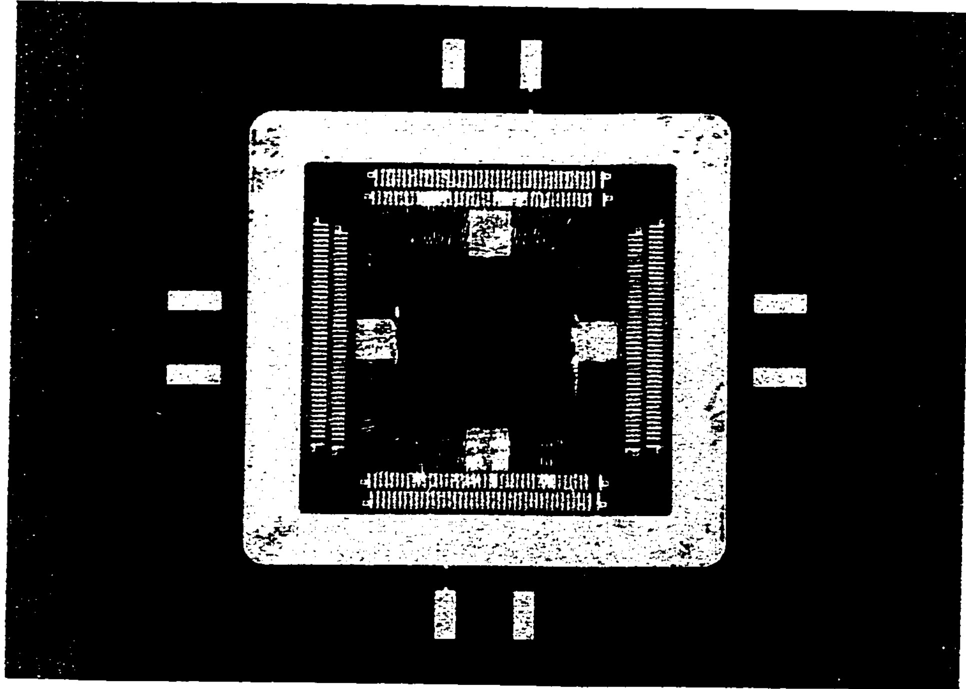

Figure 9.1 - Typical Ceramic 281-pin PGA Package with Attached Test Chip

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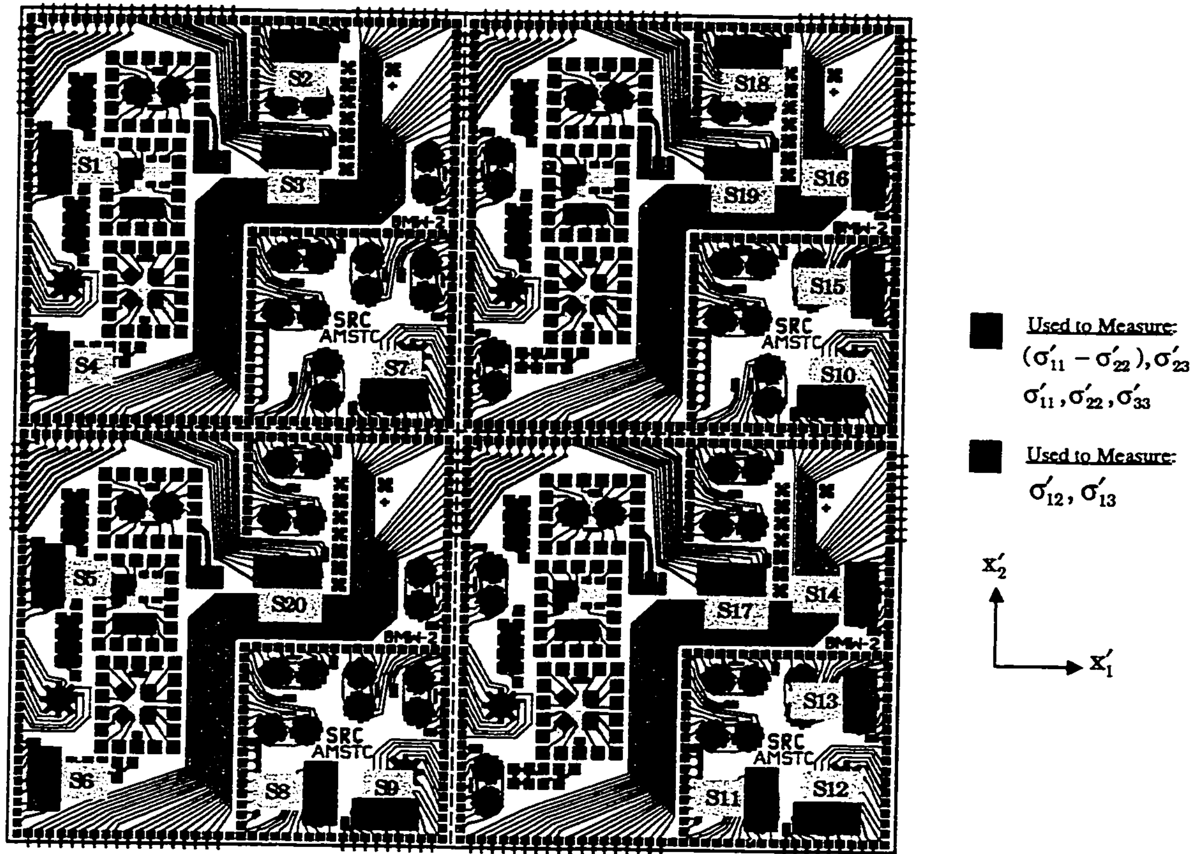

Figure 9.2 - Sensor Rosette Locations (400 x 400 mil Test Chip, PGA Study)

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changes and Eqs. (4.4, 4.5), all of the stress components at all of the rosette sites on the die surface have been calculated during the entire experimental process.

9.3 Room Temperature Stresses

After the completion of die attachment cure, the packages were allowed to cool from the curing temperature to room temperature. The room temperature sensor resistances were then measured, and the stresses were calculated using the original (wafer level) and final (packaged) die sensor resistances, and Eqs. (4.4, 4.5). Since both of these resistor measurements and the calibration of the piezoresistive coefficients were done at room temperature (23 °C), any thermal errors will be minimized. Figure 9.3 and Figure 9.4 show the measured data for the in-plane shear stress σ'_{12} and in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$), respectively. Each of the small squares in these diagrams locates a sensor rosette site. The color of a given square represents the average room temperature experimental value of the stress at the rosette site considering all of the tested samples (the square is colored to scale of the indicated legend).

The highest stress values were found in the packages assembled with Adhesive F. Adhesives A and B are both silver-filled glass based die attachment materials. Similar stress distributions on the surface of the die were found for these two adhesives because they share similar mechanical properties, curing conditions, etc. Also, the magnitudes of the normal stress difference values for adhesives A, B, and F were found to be considerably higher than those found for more conventional die attachment materials [23, 117]. The stress magnitudes were lower for the other three die attachment materials,

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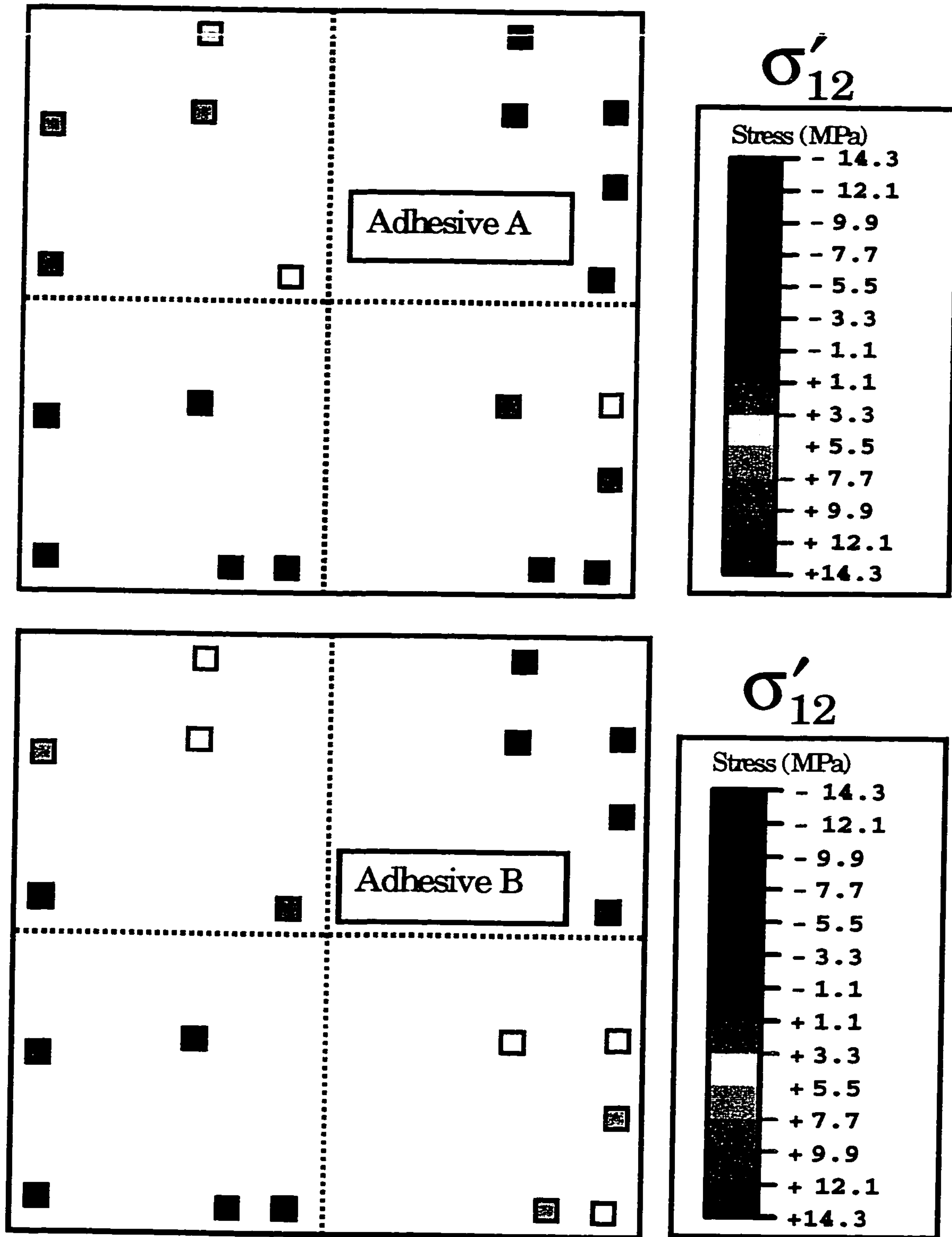

Figure 9.3 - Measured In-Plane Shear Stress Distributions (PGA Study)

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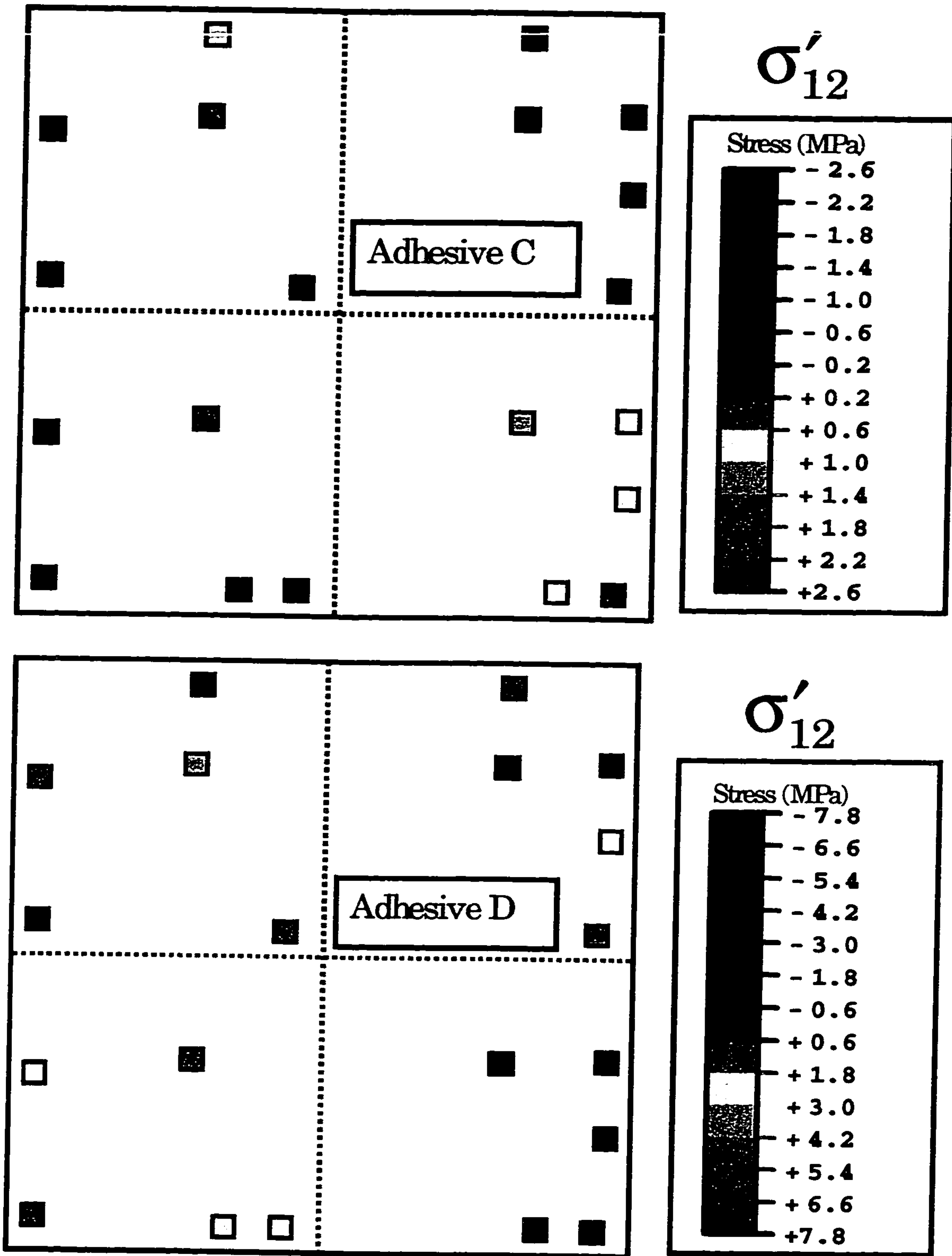

Figure 9.3 - Measured In-Plane Shear Stress Distributions (PGA Study) (Continued)

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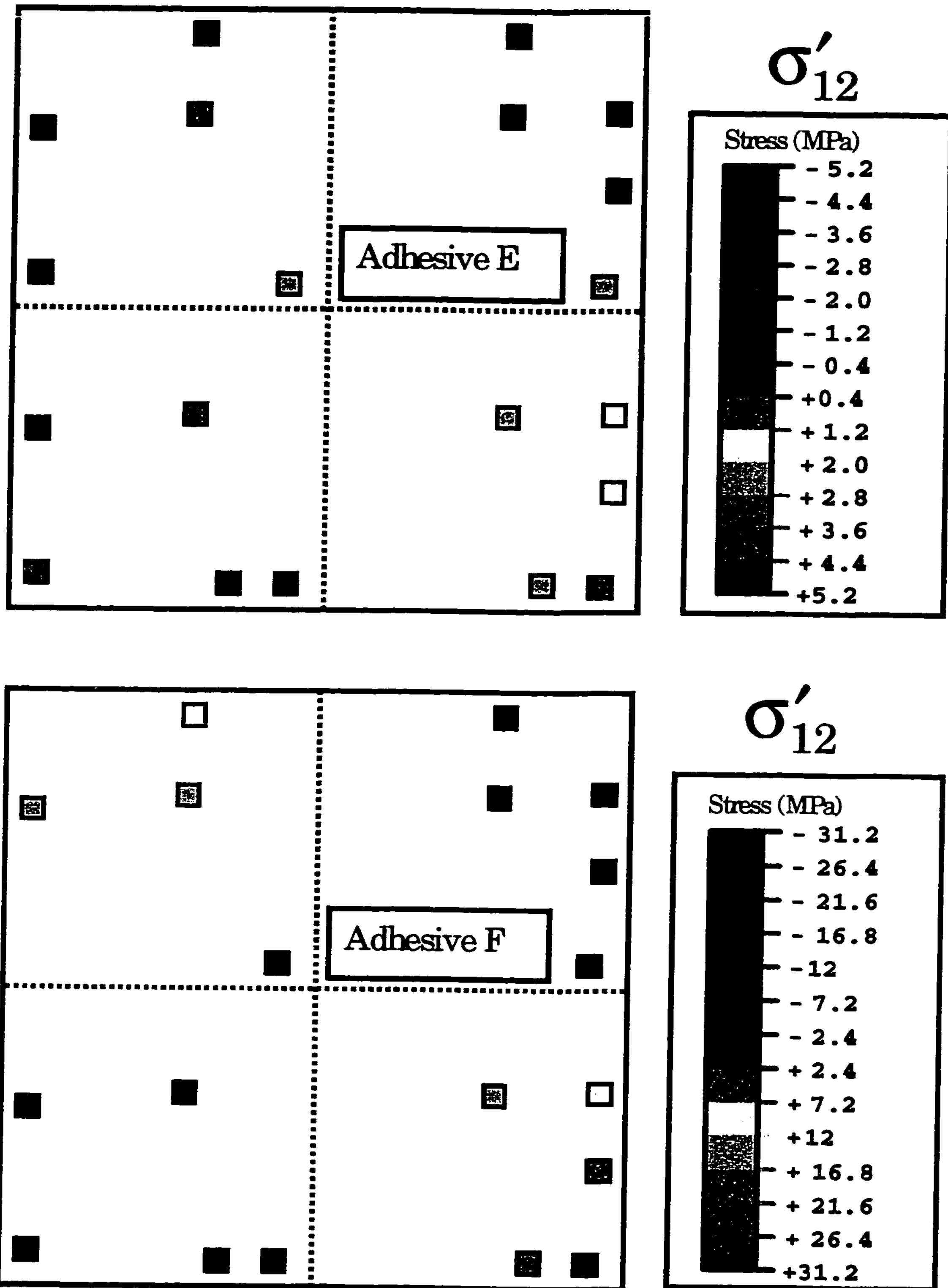

Figure 9.3 - Measured In-Plane Shear Stress Distributions (PGA Study) (Continued)

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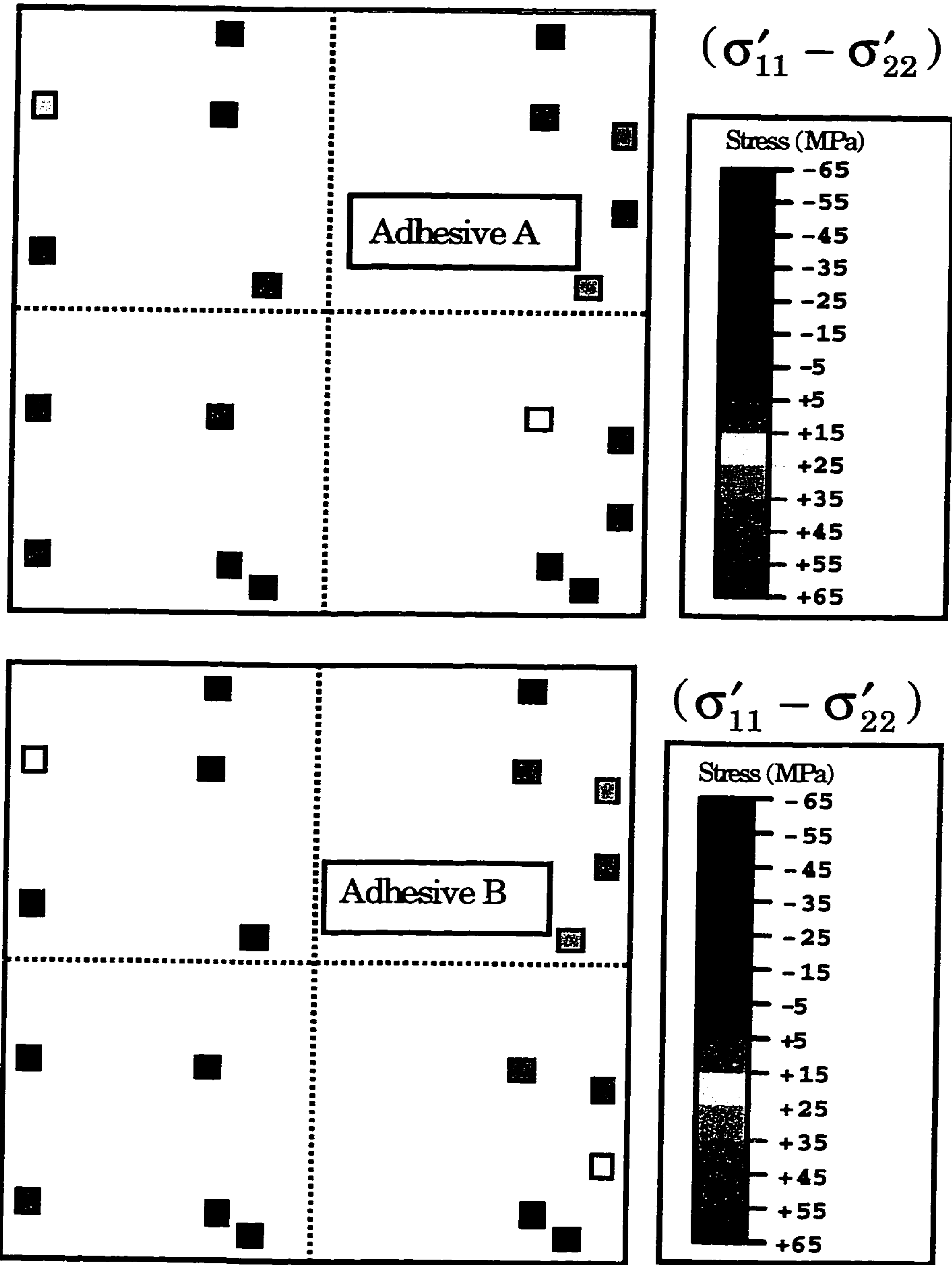

Figure 9.4 - Measured In-Plane Normal Stress Difference Distributions (PGA Study)

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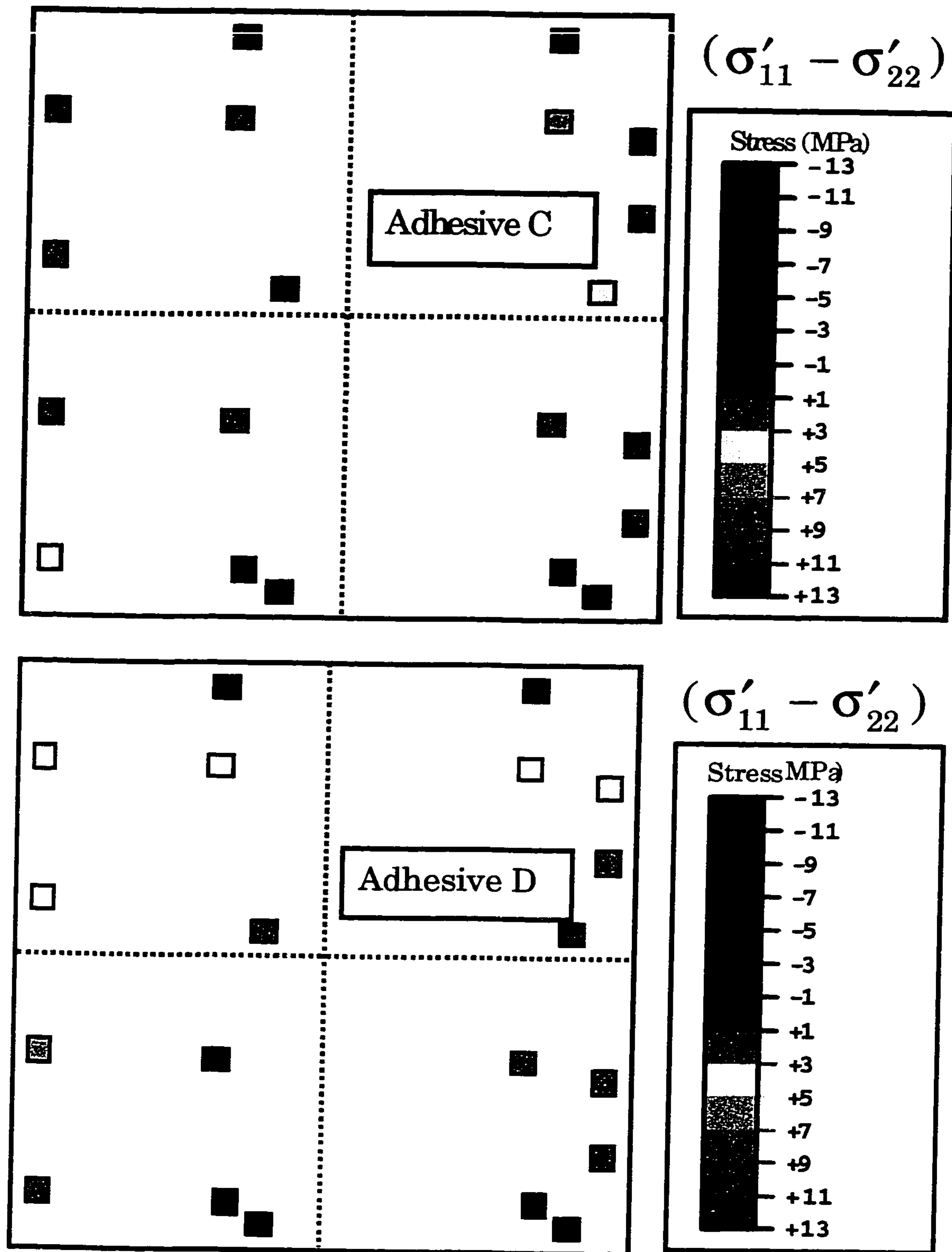

Figure 9.4 - Measured In-Plane Normal Stress Difference Distributions (PGA Study) (Continued)

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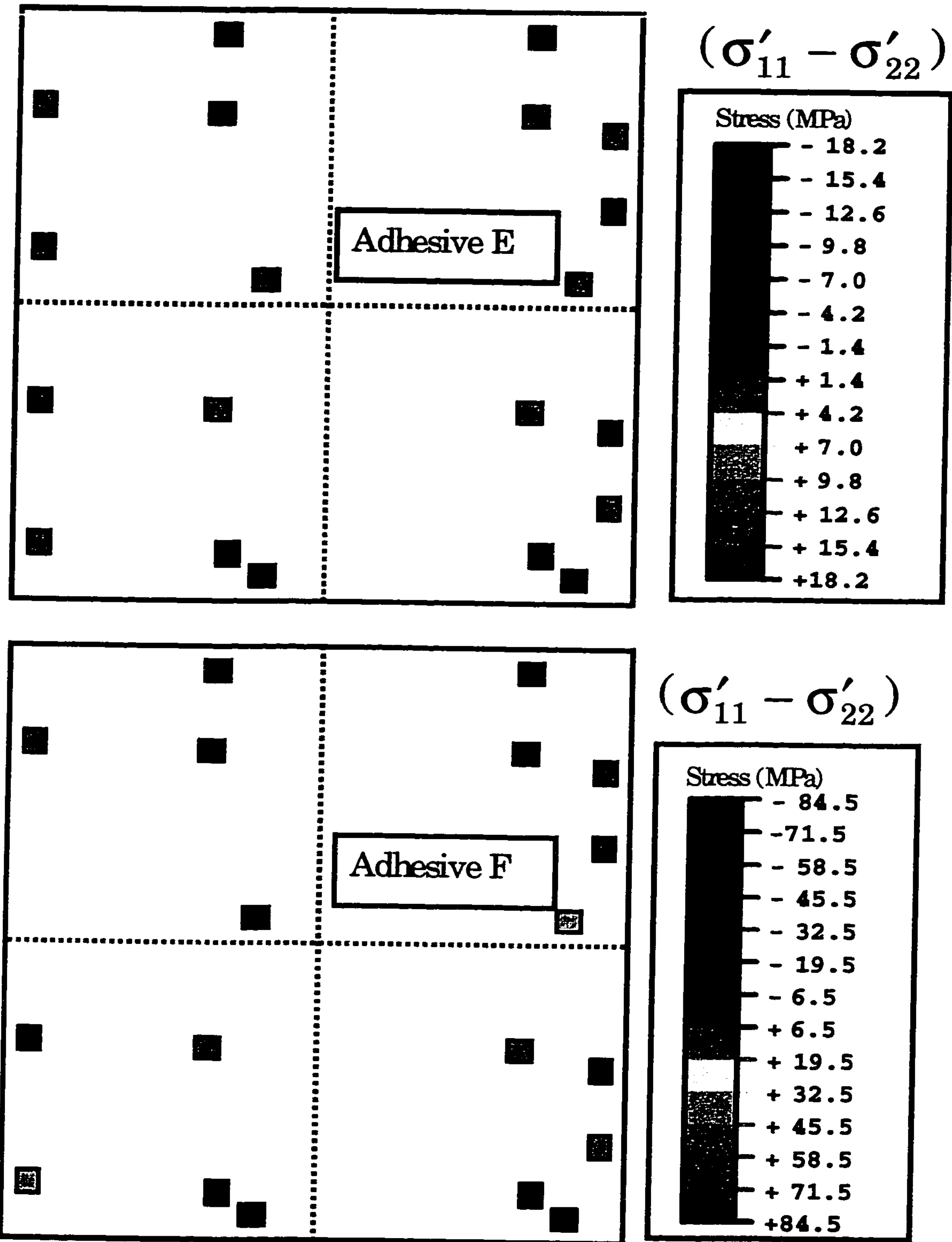

Figure 9.4 - Measured In-Plane Normal Stress Difference Distributions (PGA Study) (Continued)

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even though the CTE's of adhesives C, D, E are larger than those of adhesive A, B, and F. This is because adhesives A, B, and F have higher elastic moduli, higher glass transition temperatures, and higher curing temperatures than the other adhesives. Maximum room temperature stress values for each die attachment material are given in Table 9.2.

Material	$\lvert\sigma'_{12}\rvert$	$\lvert\sigma'_{11}-\sigma'_{22}\rvert$
A	13.3	48.4
B	7.1	57.3
C	2.5	12.6
D	7.6	10.2
E	4.3	17.0
F	27.9	83.2

Table 9.2 - Maximum Stress Values at Room Temperature (MPa)
(PGA Study)

The experimental results for adhesives A and B have been also evaluated through correlation with the predictions of three-dimensional finite element simulations of the packaging process. In the finite element models, the materials were modeled as linear elastic. However, using temperature dependent and time dependent die attachment material behavior can generate more accurate finite element results. Figure 9.5 shows a quarter model/mesh of the PGA with a test chip in the cavity. The die was assumed to be stress free at the glass transition temperature of the given die attachment material, and cooling from the glass transition temperature to room temperature was simulated. Figures 9.6 and 9.7 show finite element predictions for the die surface

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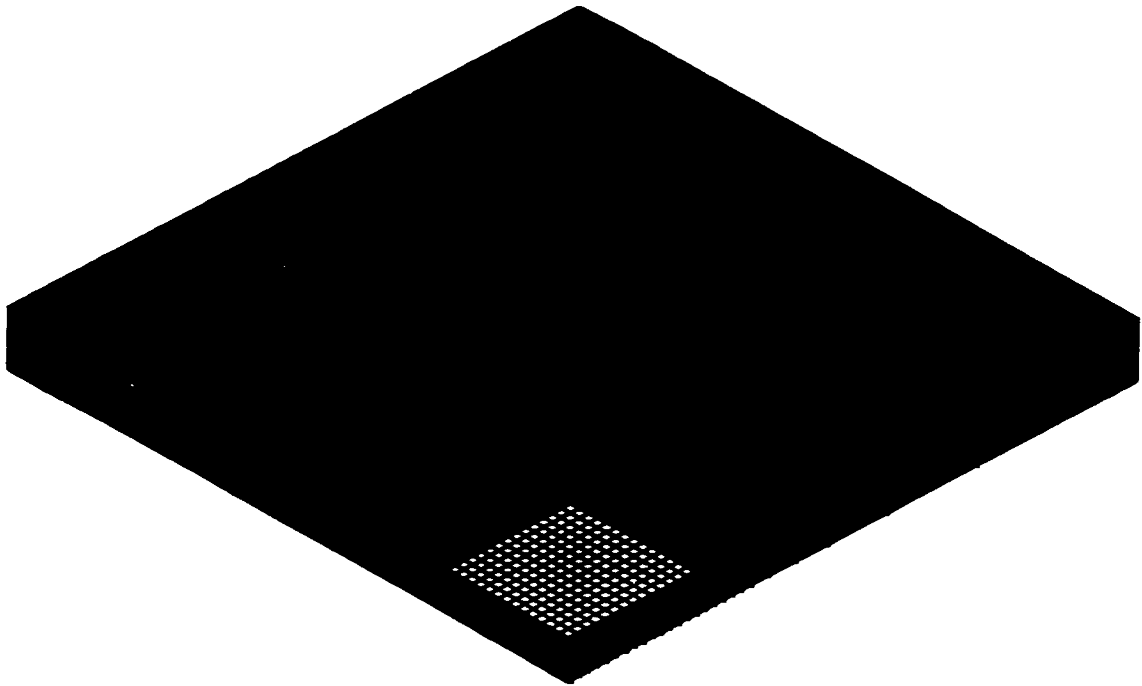

Figure 9.5 - Finite Element Mesh for the PGA Package (One Quarter Model)

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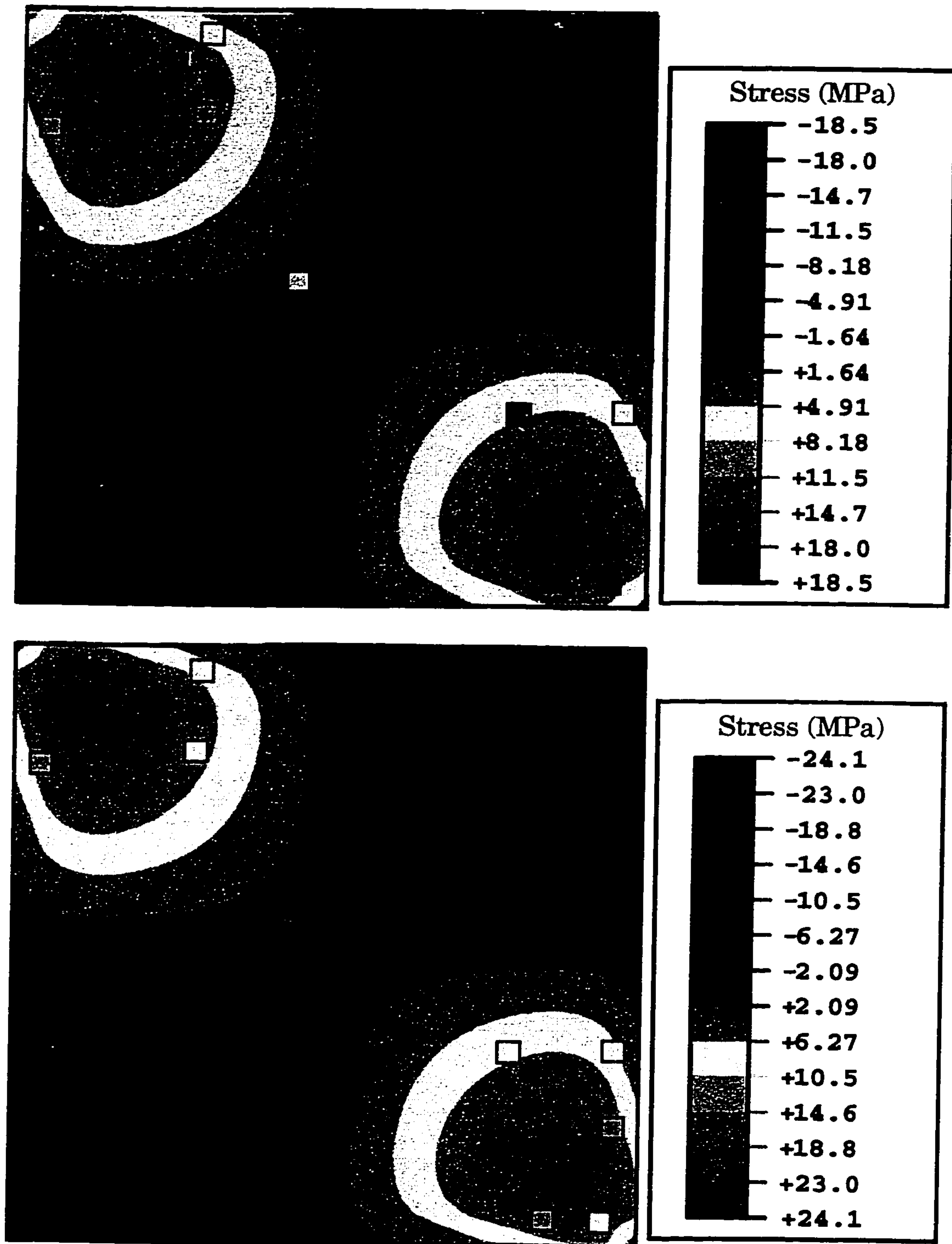

Figure 9.6 - In-Plane Shear Stress Contour Maps Predicted by Finite Element Analysis and Experimental Data (PGA Study)

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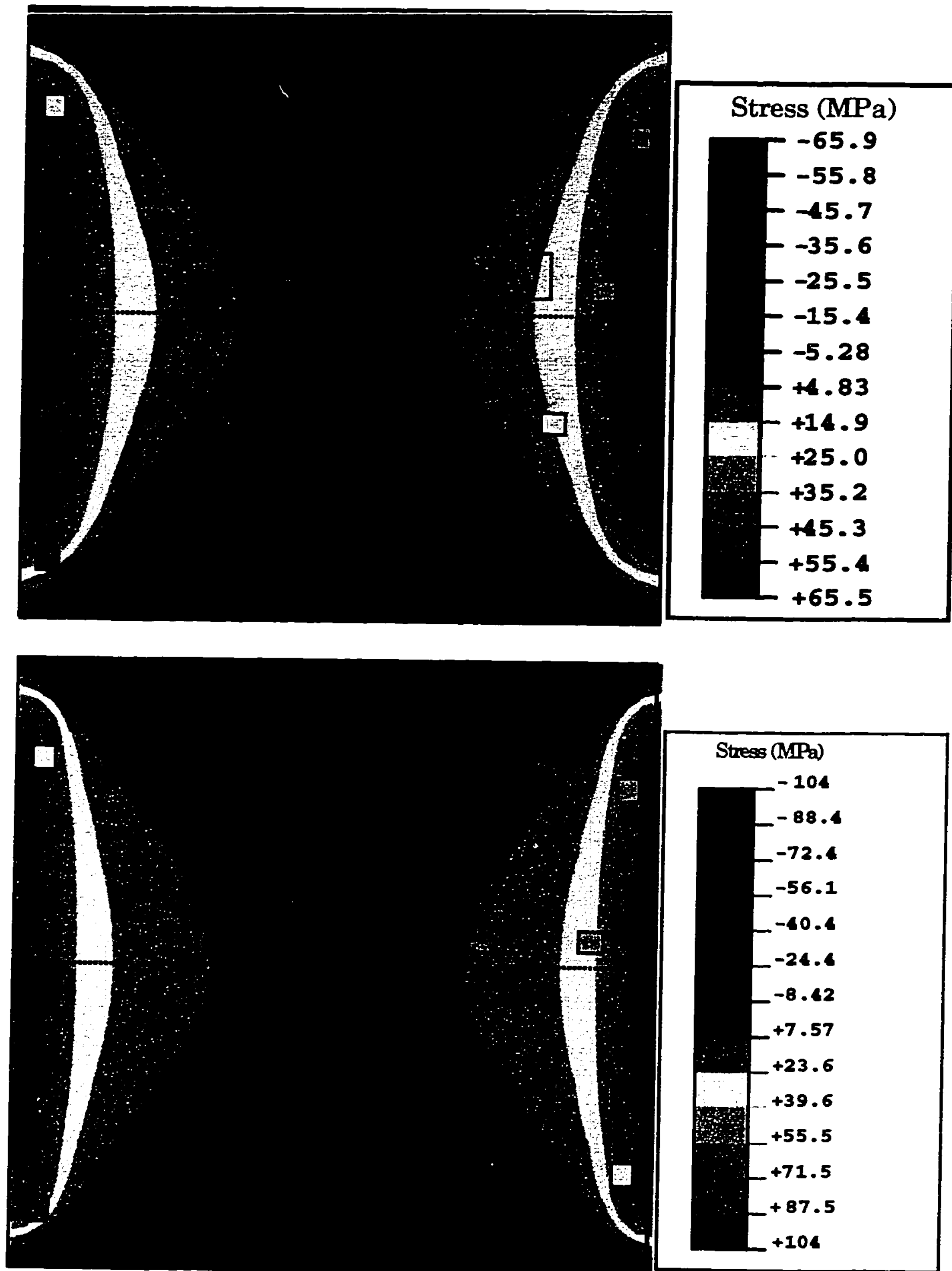

Figure 9.7 - In-Plane Plane Normal Stress Difference Contour Maps Predicted by Finite Element Analysis and Experimental Data (PGA Study)

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distributions of the in-plane shear stress (σ'_{12}) and in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$), respectively.

From both the die stress measurement and numerical prediction results, the magnitudes of the in-plane normal stress differences were found to be significantly higher than those of the in-plane shear stresses. It can be seen from the die stress measurements that the normal stress differences are higher for Adhesive B if only high stress values are compared. The finite element predictions also show the same trend. Most of the in-plane shear stress values are small, and no significant differences between the results for the two adhesives were observed. The finite element predictions show slightly higher shear stresses with Adhesive B. All of the measured stresses show the same trends and numerical signs as the distributions predicted by finite element analysis. However, the finite element simulations over predict both normal and shear stresses due to the fact that the non-linear time dependent die attachment material behavior (e.g. creep) was neglected, and that temperature dependent material properties were not included in the model. The finite element model predictions were used to show the proper signs and approximate trends of the various stress component distributions, so that the experimental data could be better understood.

It should be noted that the out-of-plane stresses in this application are theoretically zero, since the sensor side of the die is a traction free surface. This fact was verified experimentally, as the stress sensor data indicated that values of the out-of-plane shear stresses were all negligible (0-3 MPa) for all die attachment materials.

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9.4 Stress Variation with Temperature

After completion of the die surface stress measurements at room temperature, stress variation in the packages due to temperature changes was investigated for die attachment materials A-E. Such studies are useful for expanding our understanding of package structural behavior. For each of the adhesive materials, two PGA specimens were subjected to a slow temperature change from –60 °C to 100 °C. Each specimen was placed in a thermal chamber, and the temperature was first lowered to -60 °C. Resistance values were then monitored continuously as the temperature was increased, and data were recorded for temperature increments of 5 °C. The specimens were held at a given temperature for two minutes before resistance measurements were taken. The stresses on the die surface were extracted as a function of temperature using Eqs. (4.4, 4.5) and the measured resistor data. Higher temperature tests were not performed due to limitations of the testing socket. In the stress calculations, it was assumed that the piezoresistive coefficients were approximately independent of temperature.

Typical in-plane shear stress and normal stress difference data as a function of temperature are presented in Figure 9.8 and Figure 9.9, respectively. Considering locations of significant stress magnitude, site 12 was selected to demonstrate the in-plane shear stress behavior, and site 4 was chosen to illustrate the in-plane normal stress difference variation with temperature. In both cases, raising the temperature from room temperature decreased the magnitudes of the stress components for all five adhesives. This is as expected, since as the temperature becomes nearer to the cure temperature of the die adhesive, the stresses should approximately approach zero (because the cure

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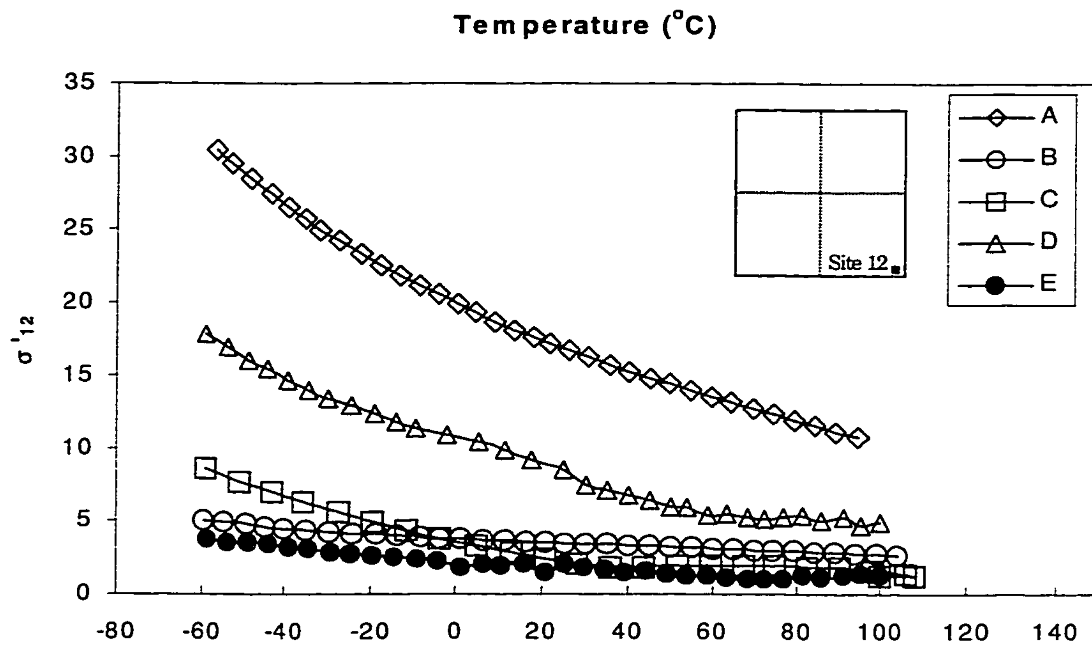

Figure 9.8 – Variation of Die Attachment Stress with Temperature (PGA Study, Sensor at Site 12)

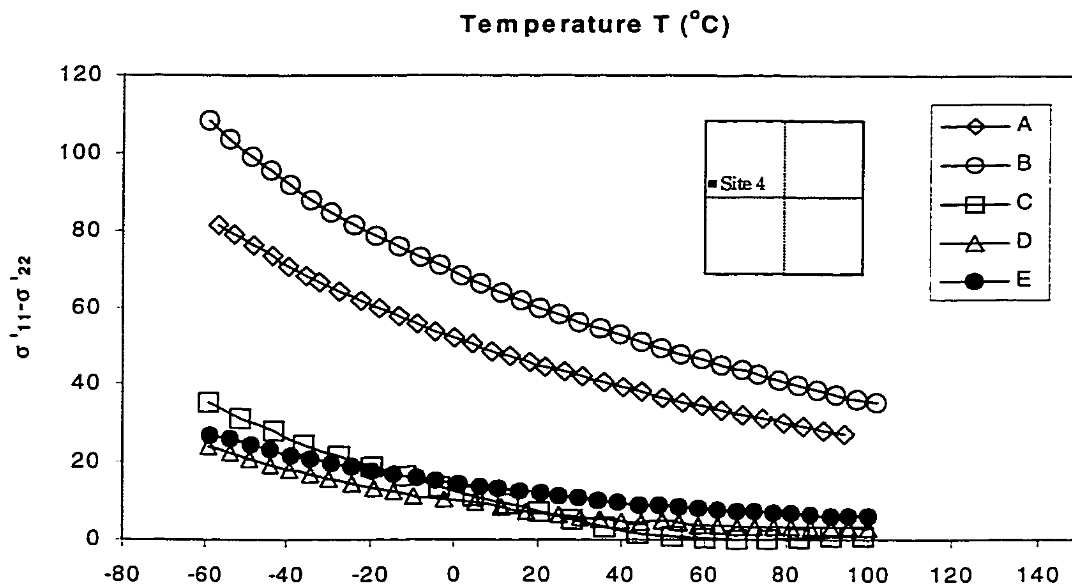

Figure 9.9 – Variation of Die Attachment Stress with Temperature (PGA Study, Sensor at Site 4)

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temperature is nearly the "relaxed" configuration of the structure). Likewise, the stress levels increase at lower temperatures, because the material expansion mismatches become larger due to the higher temperature changes from the "relaxed" configurations of the packages at their die attachment adhesive curing temperatures. At T = –60 °C, the normal stress difference levels on the die surface for adhesives A and B have become much larger (greater than 100 MPa) than those experienced in conventional plastic encapsulated packages [23, 117].

9.5 Aging and Thermal Cycling Reliability Tests

After the initial measurements described above, stringent qualification reliability testing was carried out to evaluate the capability of the die attachment adhesives A-E to survive a variety of severe environments. The PGA samples for each adhesive were separated into two groups. The first half were subjected thermal aging tests and the second half to thermal cycling tests. A fixed temperature of 260 °C was selected for thermal aging tests. The thermal cycling tests were performed with a temperature variation from -55 °C to 260 °C. A ten-minute dwell was utilized at the high and low temperature extremes, with a ramp rate of 20 °C/minute in the transition periods. Figure 9.10 illustrates the temperature profile used in the thermal cycling tests.

Three rounds of aging tests were performed. The first test consisted of 500 hours of aging (referred to as Aging #1), the second test consisted of a further 500 hours of aging (referred to as Aging #2), and the third test consisted of another 1000 hours of aging (referred as Aging #3). After each aging experiment, the samples were taken out of the

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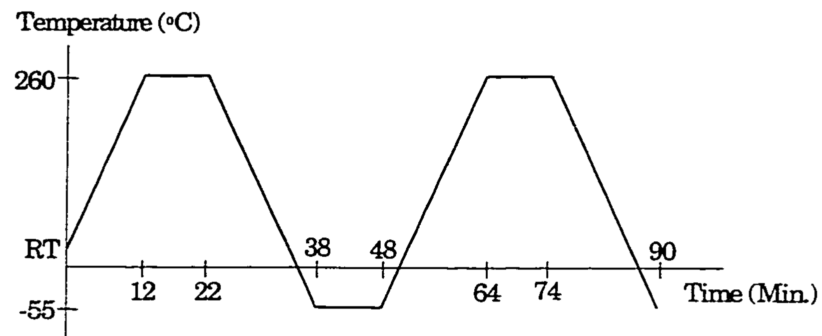

Figure 9.10 - Thermal Cycling Temperature Profile

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oven and the resistances of all the sensors on the test die were recorded at room temperature. The stresses present after each aging test were then extracted by using Eqs. (4.4, 4.5). Figure 9.11 shows the effects of thermal aging on the die surface normal stress difference for five of the die attachment adhesive materials (A-E). Figure 9.12 shows the thermal aging results of die surface in-plane shear stress for die attach adhesive materials (A-E). After the first aging test, the stress magnitudes increased for some adhesives (Adhesives C, D, and E) while it decreased for other adhesives (Adhesives A and B). The stress magnitudes were seen to drop for all die attachment materials during the second stage of the aging experiments. During the third round of aging, the stresses remained fairly constant for all adhesives. Stress decrease/relief or change to opposite sign during aging is expected due to creep of the die attachment adhesive and/or due to the possible occurrence of delaminations or cracking of the adhesives. Figure 9.13 shows typical cracking which occurred in the die attachment adhesives during the thermal aging and thermal cycling tests.

The soak temperature for the thermal aging tests was 260 °C, which is higher than the glass transition temperature (T_g) of adhesives C, D, and E; but less than the T_g of adhesives A and B. Thus, the increase in the observed die stress magnitudes during the first aging for some of the attachment materials is thought to be due to incomplete curing of the adhesives. It is hypothesized that adhesives C, D, and E became further cured during the first aging tests, leading to increases in adhesive stiffness and higher die stresses upon temperature change.

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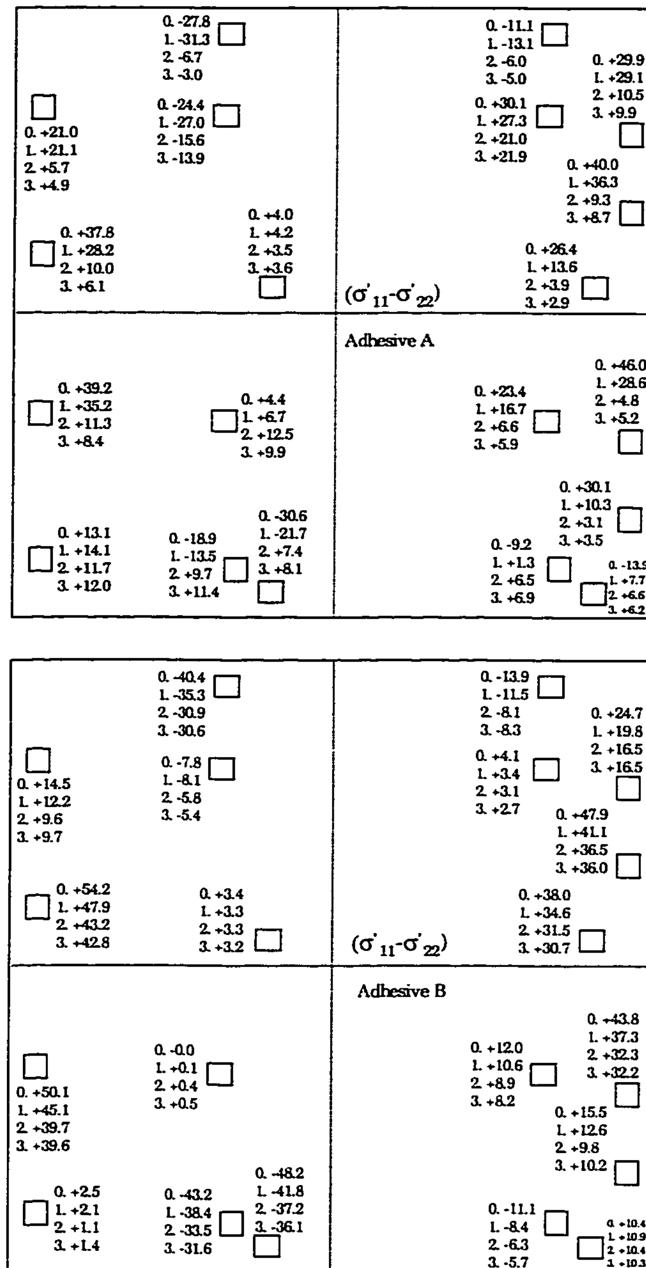

0: Before Aging
1: After Aging #1
2: After Aging #2
3: After Aging #3

Figure 9.11 - Effects of Thermal Aging on Die Surface Stresses (In-Plane Normal Stress Difference in MPa, PGA Study)

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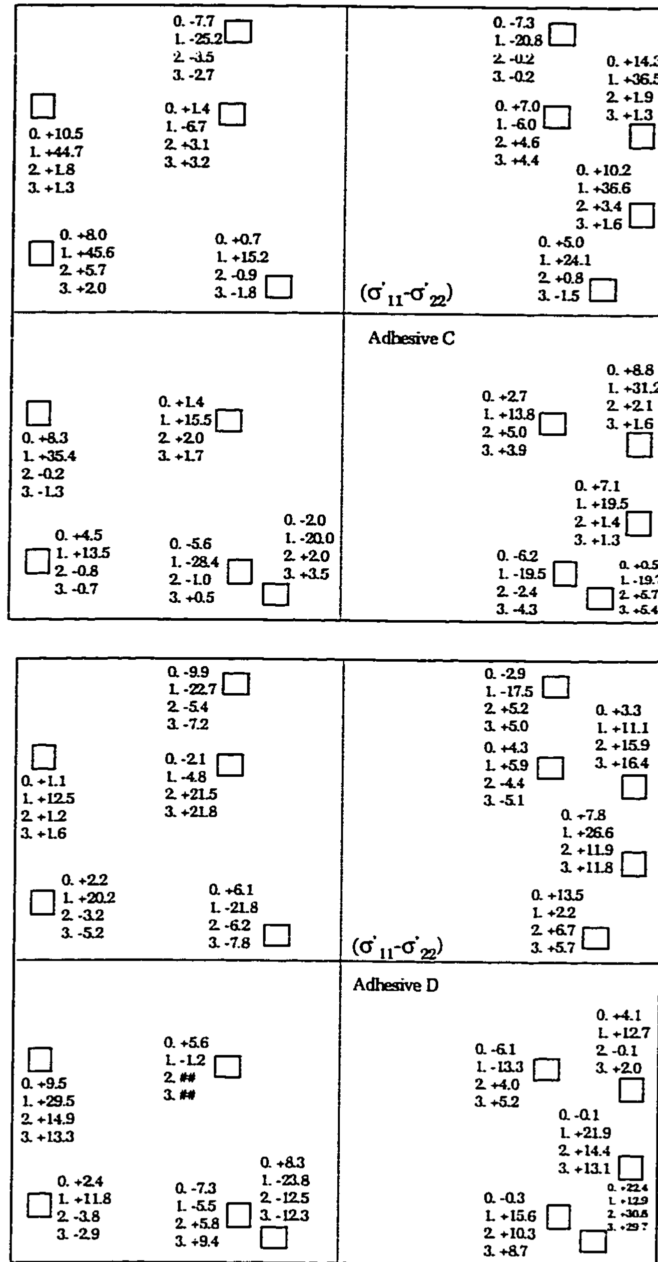

0: Before Aging
1: After Aging #1
2: After Aging #2
3: After Aging #3

Figure 9.11 - Effects of Thermal Aging on Die Surface Stresses (In-Plane Normal Stress Difference in MPa, PGA Study) (Continued)

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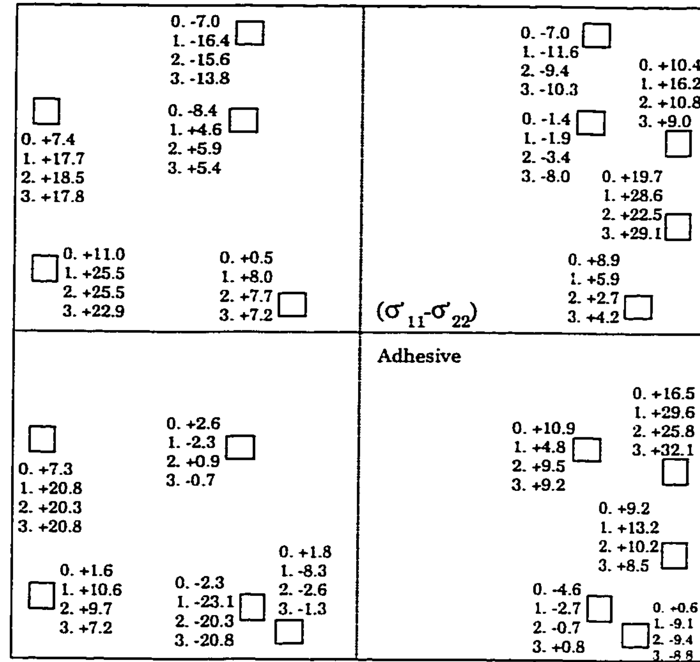

0: Before Aging
1: After Aging #1
2: After Aging #2
3: After Aging #3

Figure 9.11 - Effects of Thermal Aging on Die Surface Stresses (In-Plane Normal Stress Difference in MPa, PGA Study) (Continued)

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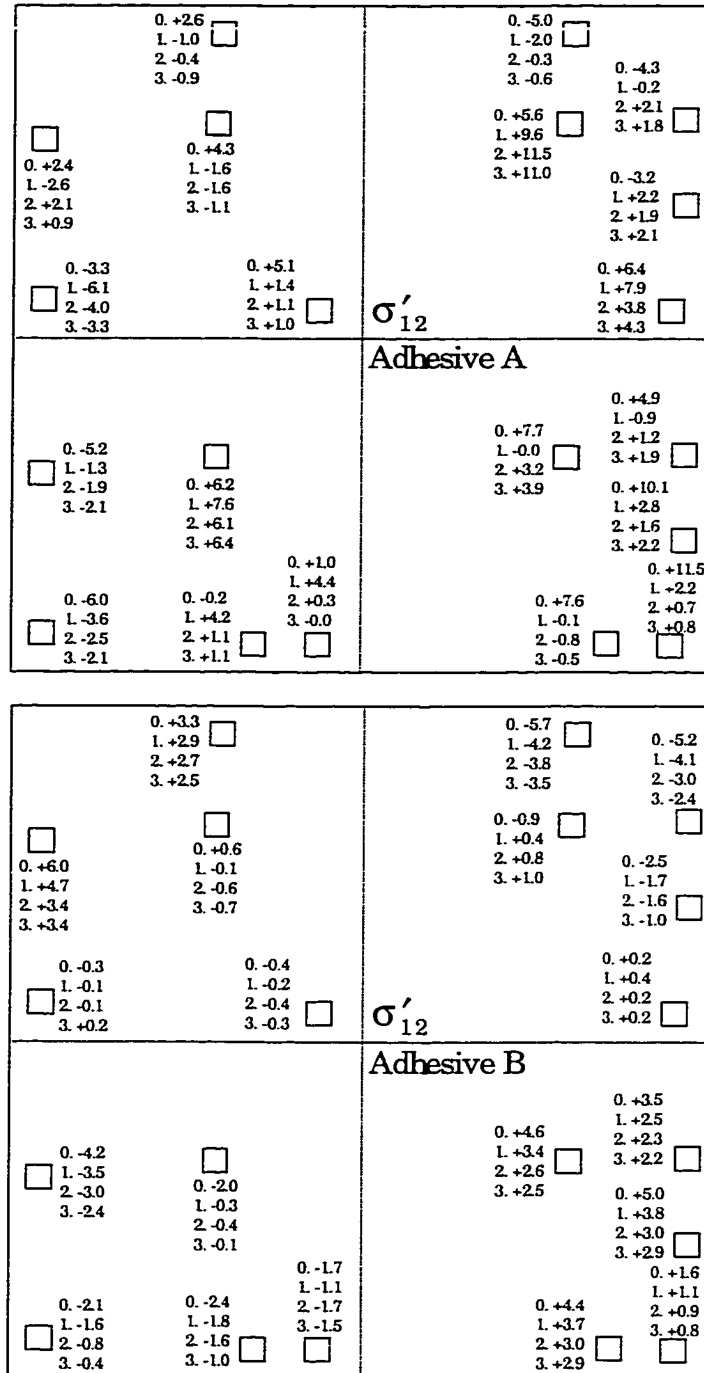

0: Before Aging
1: After Aging #1
2: After Aging #2
3: After Aging #3

Figure 9.12 - Effects of Thermal Aging on Die Surface Stresses
(In-Plane Shear Stress in MPa, PGA Study)

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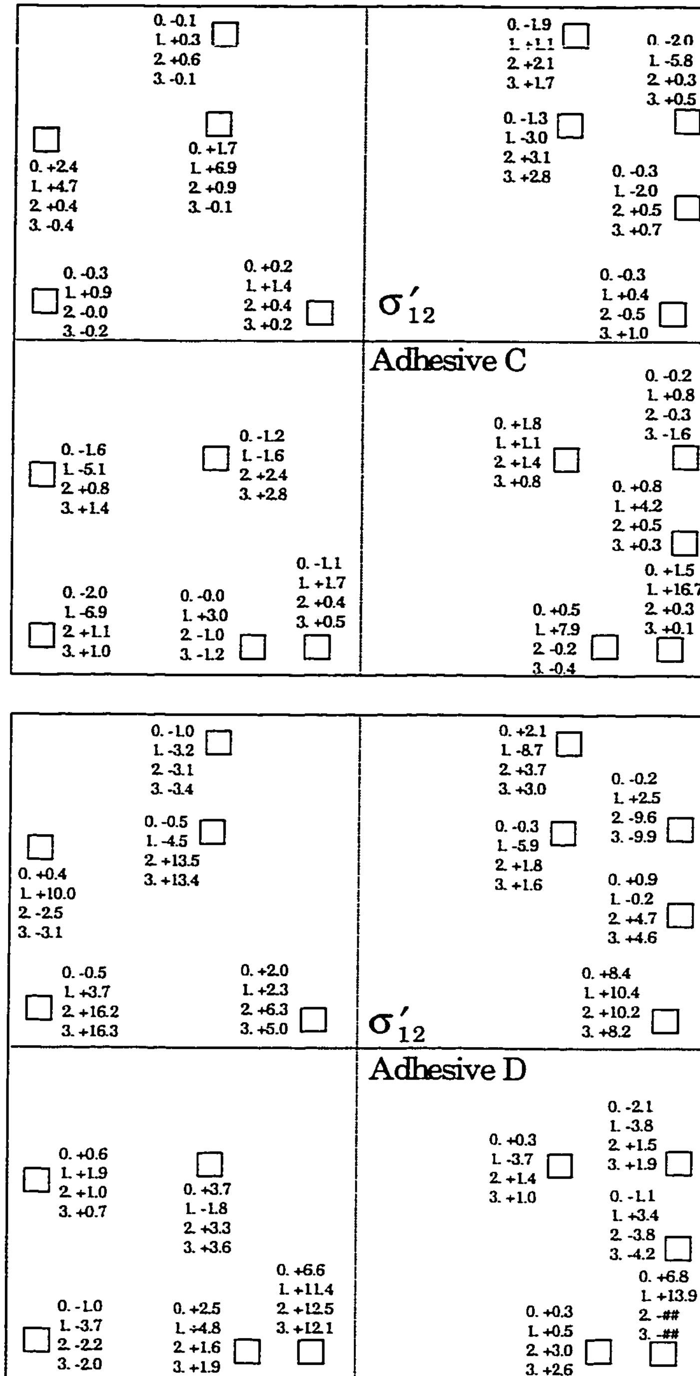

0: Before Aging
1: After Aging #1
2: After Aging #2
3: After Aging #3

Figure 9.12 - Effects of Thermal Aging on Die Surface Stresses
(In-Plane Shear Stress in MPa, PGA Study)
(Continued)

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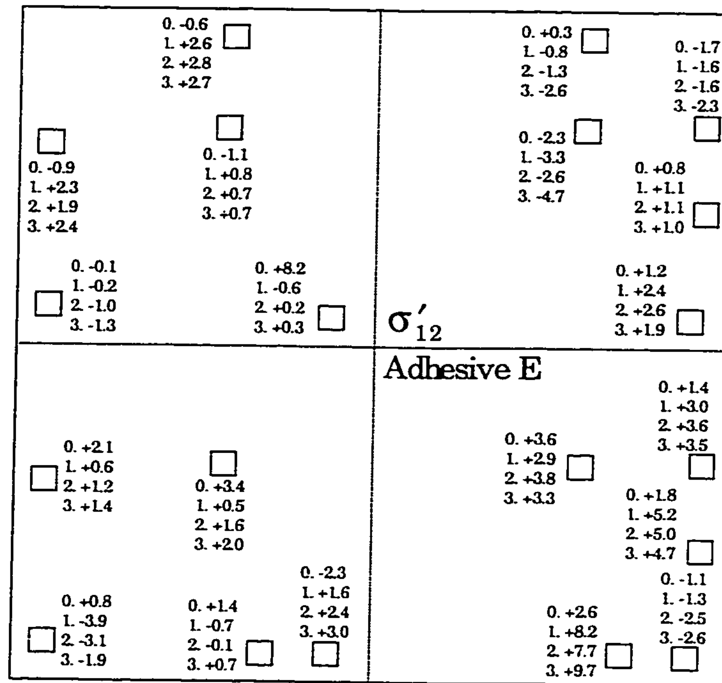

0: Before Aging
1: After Aging #1
2: After Aging #2
3: After Aging #3

Figure 9.12 - Effects of Thermal Aging on Die Surface Stresses (In-Plane Shear Stress in MPa, PGA Study) (Continued)

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Figure 9.13 - Typical Cracking and Delamination of a Die Attachment Adhesive after Reliability Testing

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The thermal cycling tests were also performed in three stages, which consisted 300 thermal cycles for both Cycling #1 and Cycling #2, and 400 thermal cycles for Cycling #3. Room temperature die stresses were evaluated after each stage of thermal cycling using the measured sensor resistances (see data in Figure 9.14 and 9.15). Analogous to the aging results, the same types of increases and decreases in the stress magnitudes were observed for the various die attachment adhesives.

Tables 9.3 and 9.4 summarize the results from the reliability testing. When only small changes were found in the die stress values during a reliability test, the samples were characterized as "Survived". For large stress changes (usually the stress magnitudes dropped to near zero), the samples were characterized as "failed" since the integrity of the die attachment adhesive was lost. Adhesives B, D, and E survived the entire thermal aging testing, while adhesives A and C survived only Aging #1. Adhesives C, D, and E performed best in the thermal cycling tests, although all adhesives failed by the end of the testing. Due to the large thermal stresses and fatigue, adhesive A and B failed much earlier. For adhesive E, the sensors themselves were found to have failed at most of the locations after cycling #3, indicating adhesion loss that lead to die movement and broken wire bonds.

Silver filled glasses (adhesives A and B) were found to survive well in a constant high temperature environment, while delamination or other failures occurred during thermal cycling. The relatively high CTE's and elastic moduli could be blamed for the bad adaptability of these adhesives to cyclic temperature changes. It is also obvious that adhesive B behaved better than adhesive A. Polyimide pastes (adhesives C and D)

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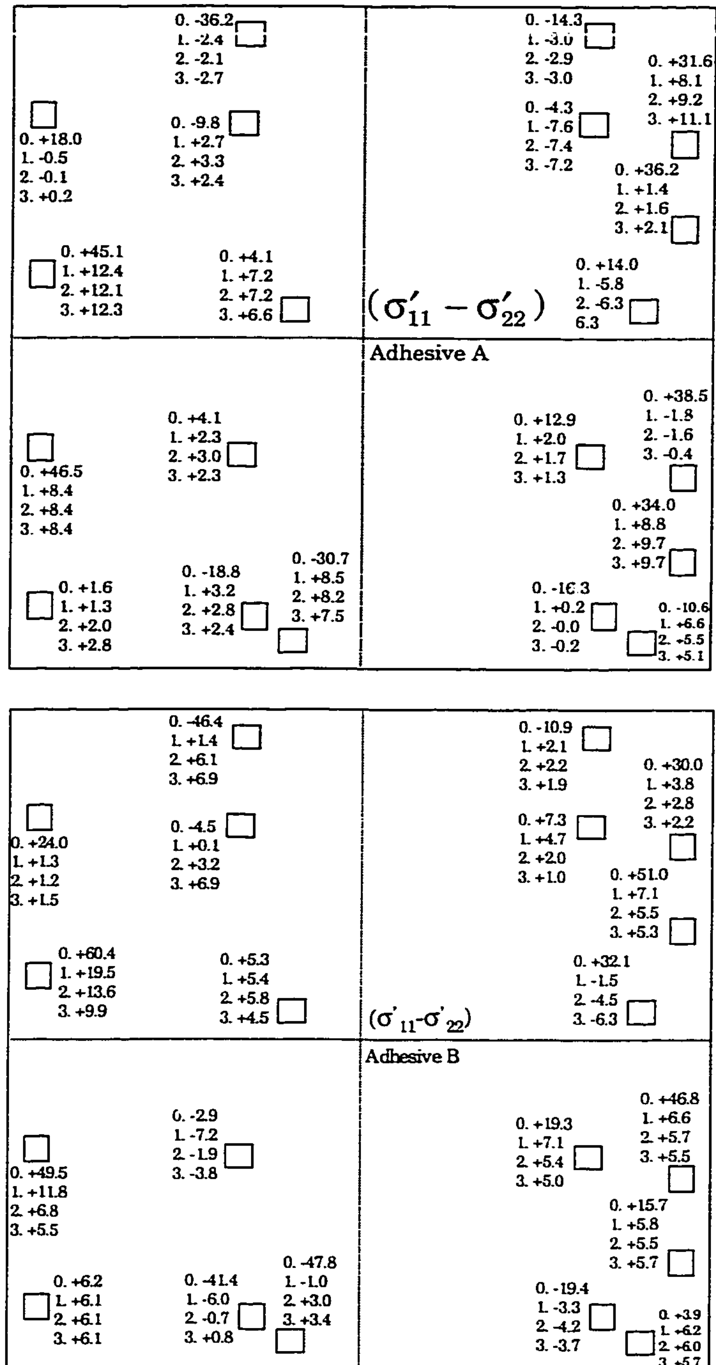

0: Before Cycling
1: After Cycling #1
2: After Cycling #2
3: After Cycling #3

Figure 9.14 - Effects of Thermal Cycling on Die Surface Stresses
(In-Plane Normal Stress Difference in MPa, PGA Study)

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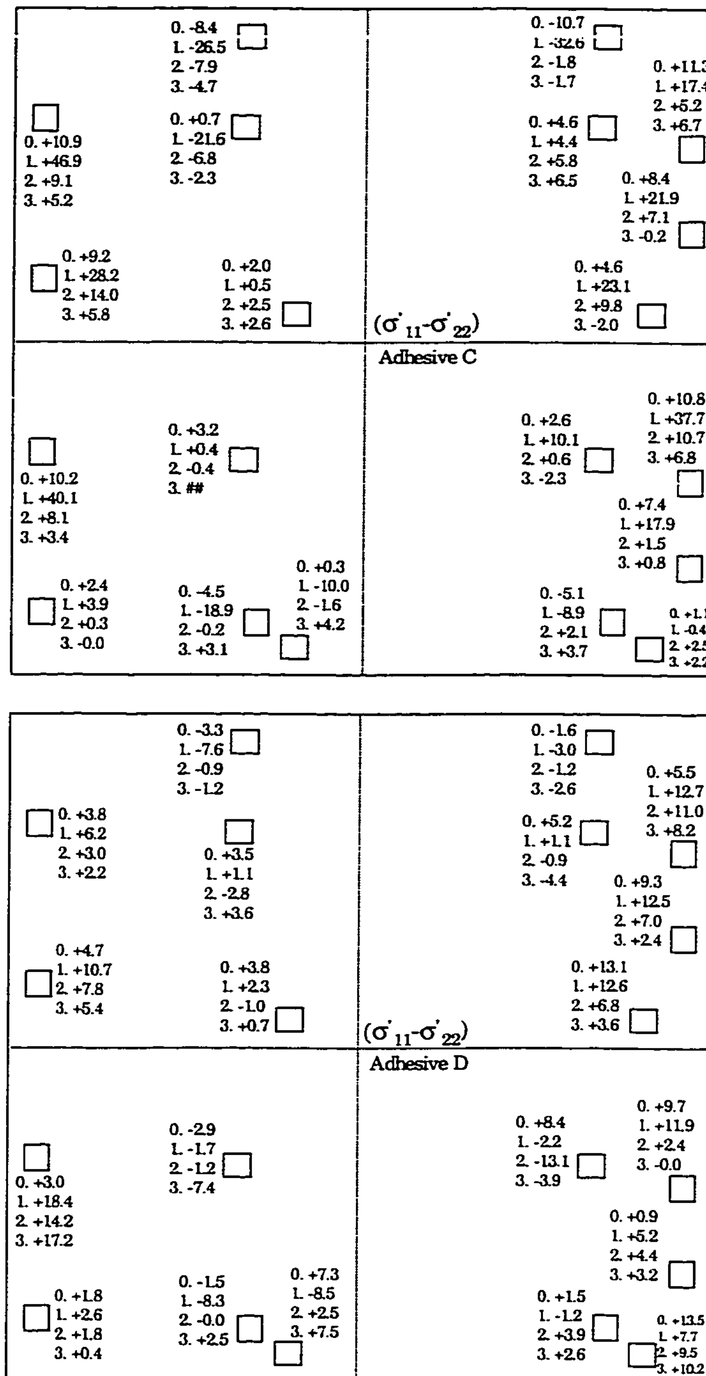

0: Before Cycling
1: After Cycling #1
2: After Cycling #2
3: After Cycling #3

Figure 9.14 - Effects of Thermal Cycling on Die Surface Stresses (In-Plane Normal Stress Difference in MPa, PGA Study) (Continued)

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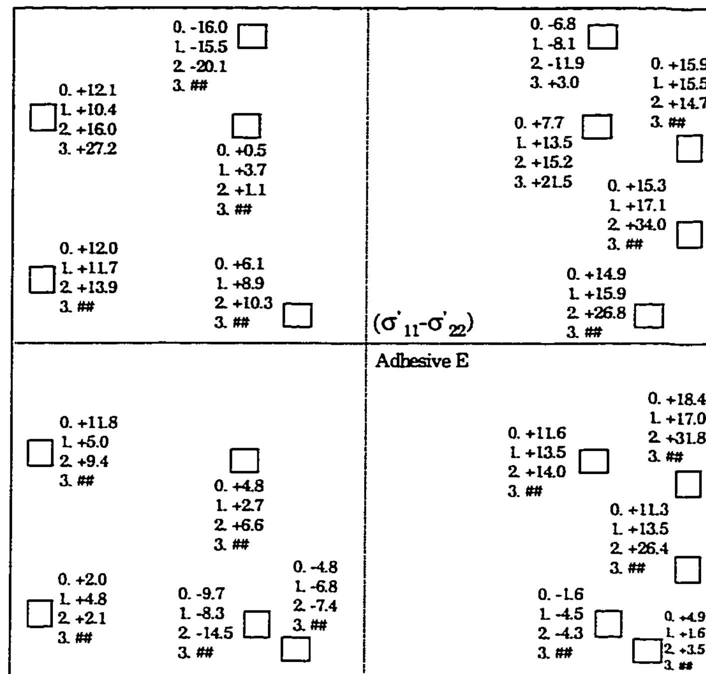

0: Before Cycling
1: After Cycling #1
2: After Cycling #2
3: After Cycling #3

Figure 9.14 - Effects of Thermal Cycling on Die Surface Stresses (In-Plane Normal Stress Difference in MPa, PGA Study) (Continued)

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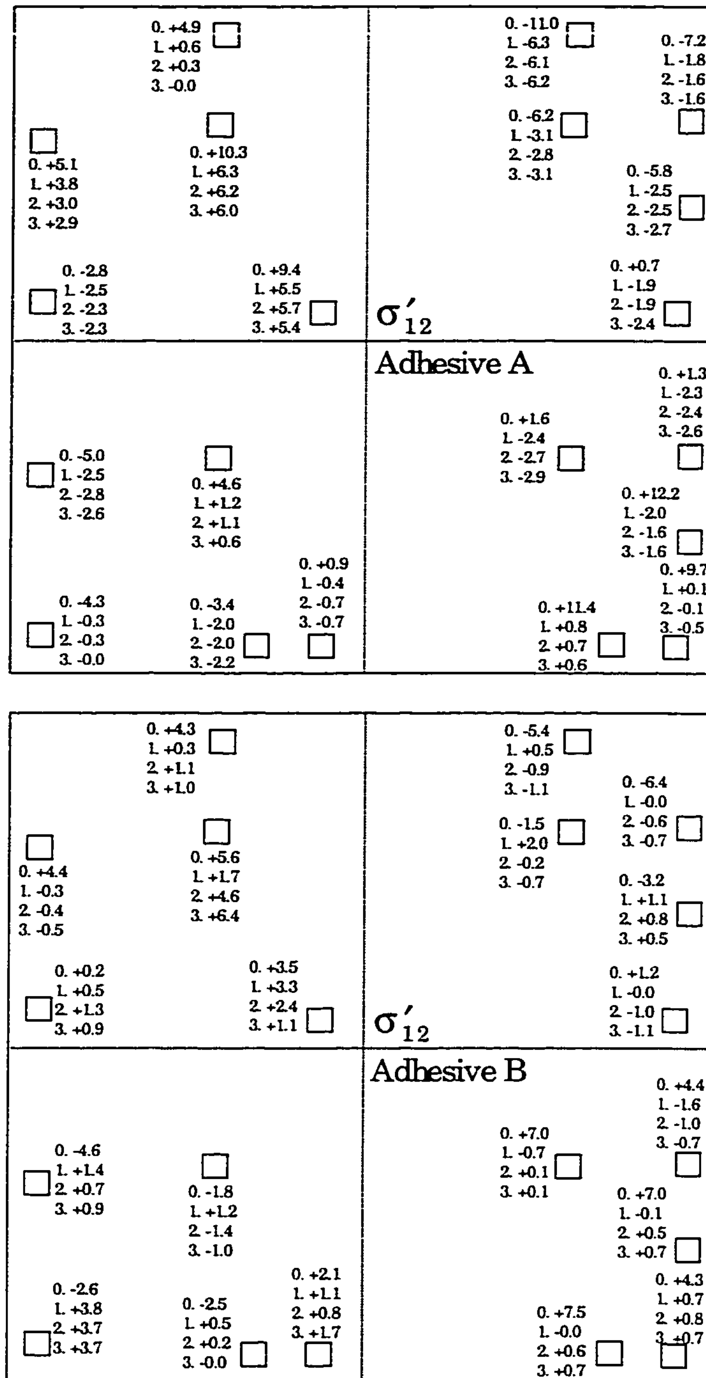

0: Before Cycling
1: After Cycling #1
2: After Cycling #2
3: After Cycling #3

Figure 9.15 - Effects of Thermal Cycling on Die Surface Stresses
(In-Plane Shear Stress in MPa, PGA Study)

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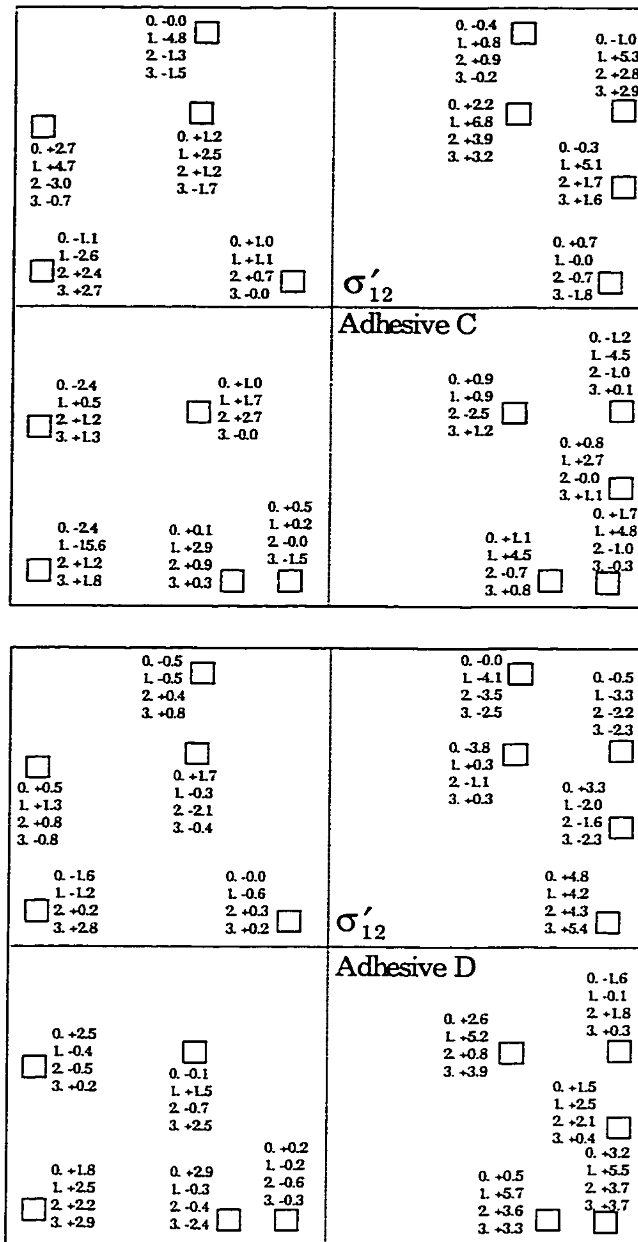

0: Before Cycling
1: After Cycling #1
2: After Cycling #2
3: After Cycling #3

Figure 9.15 - Effects of Thermal Cycling on Die Surface Stresses (In-Plane Shear Stress in MPa, PGA Study) (Continued)

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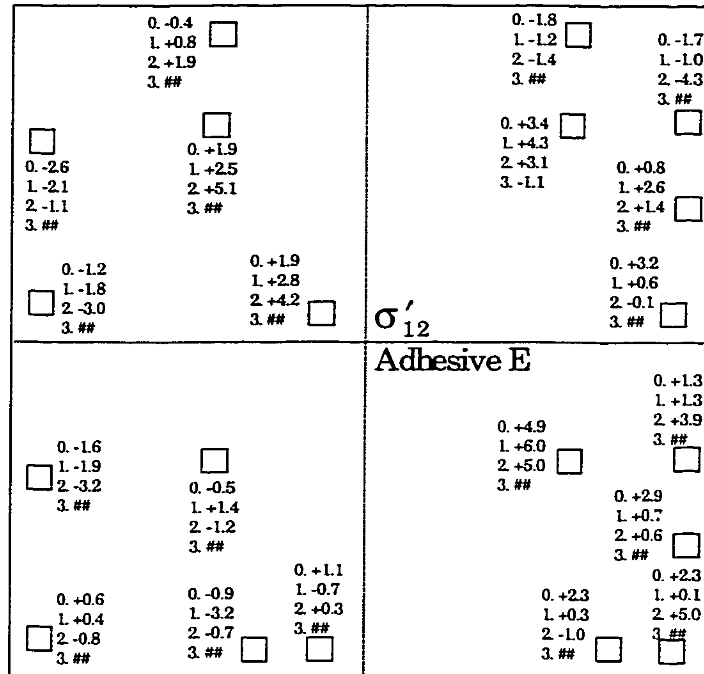

0: Before Cycling
1: After Cycling #1
2: After Cycling #2
3: After Cycling #3

Figure 9.15 - Effects of Thermal Cycling on Die Surface Stresses (In-Plane Shear Stress in MPa, PGA Study) (Continued)

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Material	Aging #1	Aging #2	Aging #3
A	Survived	Failed	Failed
B	Survived	Survived	Survived
C	Survived	Failed	Failed
D	Survived	Survived	Survived
E	Survived	Survived	Survived

Table 9.3 - Evaluation of the Die Attachment Adhesives under Thermal Aging Reliability Tests

Material	Cycling #1	Cycling #2	Cycling #3
A	Failed	Failed	Failed
B	Failed	Failed	Failed
C	Survived	Survived	Failed
D	Survived	Survived	Failed
E	Survived	Survived	Failed

Table 9.4 - Evaluation of the Die Attachment Adhesives under Thermal Cycling Reliability Tests

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responded to thermal aging and thermal cycling tests in similar ways. However, adhesive D demonstrated less stress changes during the thermal aging tests. Thus, adhesive D is recommended when compared to adhesive C. The thermoplastic film (adhesive E) survived throughout the thermal aging tests, and the first two rounds of thermal cycling tests. However, it failed catastrophically during the third round of thermal cycling tests, leading to wire bond failure. The thermoplastic film material is assumed to have fewer voids than the other materials. However, once the attachment integrity was broken, the adhesive lost its functionality quickly and thoroughly, causing the complete failure of the packages. Unusual stress values were detected at some measurement locations during the thermal aging and thermal cycling tests. Local voids or delaminations could be blamed for such stress concentrations.

9.6 Summary

High temperature die attachment effects on die stresses have been studied using special (111) silicon test chips containing an array of piezoresistive stress sensor rosettes. Calibrated and characterized test chips were attached to 281-pin PGA packages. The temperature compensated stresses were evaluated from the room temperature sensor resistance measurements after die attachment. The measured stresses show the same trends and numerical signs as the distributions predicted by finite element analysis. However, the finite element simulations over predicted the stresses due to the fact that time and temperature dependent material properties for the die attachment materials were not included in the models. Variations of the die stresses during slow temperature

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changes were also investigated. As expected, stress relief occurred as the temperature approached the glass transition temperature of corresponding adhesive. Thermal aging and thermal cycling tests were carried out to evaluate the reliability characteristics of each adhesive. A variety of results were obtained for the various adhesives, and typical data were presented.

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CHAPTER 10

SUMMARY AND CONCLUSIONS

In this work, both (100) and (111) silicon test chips containing an array of optimized piezoresistive stress sensor rosettes, which were designed and fabricated in Auburn University, have been successfully applied within several plastic encapsulated electronic packaging configurations. Calibrated and characterized (100) and (111) test chips were encapsulated in various packaging configurations. The post packaging resistances of the sensors were then recorded. These packaging resistances were monitored at room temperature, as a function of temperature excursion, or during a long term packaging reliability qualification tests (thermal cycling and thermal aging). The stresses on the die surface were calculated using the measured resistance changes and the appropriate theoretical equations. For comparison purpose, three-dimensional nonlinear finite element simulations of the plastic encapsulated packages were also performed, and the stress predictions were correlated with the experimental test chip data.

(100) silicon test chips (AAA2) containing optimized four-element dual polarity rosettes have been applied within plastic electronic packaging configurations including 44 pin Plastic Leaded Chip Carrier (PLCC) packages and 240 pin Quad Flat Packs (QFP's). In the stress studies of PLCC packages, 100 x 100 mil test chips were encapsulated. Several molding compounds were considered to compare the different stress levels by

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various encapsulants. 450 x 450 mil test chips were used in 240 pin QFP's to study stress distribution on larger die surface. Also, no delaminations between the die surface and the encapsulant occurred. The stress measurement results then served as a reference for the following stress evaluations within delaminated QFP's. For all the packaging configurations, three-dimensional nonlinear finite element simulations were performed to correlate the experimental results.

Advanced (111) silicon test chips (BMW-1 or BMW-2) comprising an array of optimized eight-element dual polarity piezoresistive sensor rosettes played a key role in recent stress assessments. 400 x 400 mil silicon test chips were encapsulated in 240 pin QFP's, 160 pin QFP's, Chip On Board (COB) packages, and 281 pin ceramic Pin Grid Array (PGA) packages. When BMW-1 test chips were used to characterize 240 pin QFP's, the presence of delaminations between the die surface and the encapsulant was explored using C-Mode Scanning Acoustic Microscopy (C-SAM). The stress distributions in delaminated packages were compared with those in non-delaminated packages. In addition, a large number of BMW2 test chips were also encapsulated in 240 pin QFP's. The room temperature stress measurements were consistent with the previous conclusions. Two molding compounds were involved in stress estimation within 160 pin QFP's. The postmolded room temperature stress results were then compared.

Die stresses in wire bonded COB packages were measured using BMW-2 silicon stress test chips encapsulated in two molding compounds. The stress sensing rosettes were characterized after die attachment, and throughout the cure cycle of the liquid encapsulant. Using the measured data and appropriate theoretical equations, the stresses at sites on the

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die surface have been calculated. Also, the stresses were studied as a function of temperature. More COB package studies were performed. In this case, a comparison of COB stress levels with convection and variable frequency microwave encapsulant curing was carried out. This comparison went through the entire packaging processes. Thermal cycling tests and moisture absorption tests were conducted for some of the COB samples. The stress variations were then obtained as a function of thermal cycles, and with the states of moisture absorption. The comparison of stress levels with two encapsulant curing methods were then made during the thermal cycling tests and moisture absorption tests.

High temperature die-attach materials were evaluated by applying BMW2 test chips to 281 pin ceramic PGA packages. Five adhesives utilized in this experiment included silver filled glass, polyimide paste, and thermoplastic film. The comparison of die stresses at room temperature caused by different die attach materials has been made. The thermal stresses on the die surface were also extracted as a function of temperature when a single thermal cycle was applied. In addition, thermal aging and thermal cycling tests were conducted for the PGA packages. Die attach materials were evaluated by the stress excursions due to these reliability tests.

Finally, nonlinear finite element simulations of 240 pin QFP's, 160 pin QFP's, COB packages, and 281 pin ceramic PGA packages were performed. Anisotropic (111) silicon material properties were used, while isotropic properties were assumed for materials other than silicon die. The materials were modeled as linear elastic, and large deformations (kinematic nonlinearities) were utilized.

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It has been proven that piezoresistive stress sensors are a powerful tool for experimental structural analysis of electronic packages. Especially, by using (111) silicon stress test chips, a complete stress state at a point on the surface of the silicon die can be extracted. The test chips are used to evaluate packaging materials such as encapsulants, die attachment adhesives, etc. They are used to investigate packaging processes such as die attachment and encapsulation. They can also be utilized to evaluate package performance during qualification reliability testing. Finally, the unique capability of measuring out-of-plane shear stresses of (111) silicon test chip offers a good chance to detect delaminations at the interface of silicon die and encapsulants above.

There are several opportunities for future work. For example, the (111) silicon test chips could be applied in flip chip packaging configurations. The stress distribution of the silicon die due to under fill and solder bumping could be explored. Also, the warpage of the silicon die could be studied by measuring the stress distribution on the backside of the die. More sophisticated finite element models could be developed by including more realistic material properties and assumptions for interfaces of dissimilar materials. Improved FEM predictions may give better correlation with experimental data. Further investigations of delamination at the interface of silicon die and encapsulant using (111) silicon test chip are also needed.

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APPENDICES

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APPENDIX A

A VISUAL BASIC PROGRAM FOR GPIB CONTROLLED RESISTANCE MEASUREMENTS OF BMW-2 SENSOR ROSETTE IN COB STUDIES

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s2n3

15858.25

15858.06

0.4521432

1

21.6665588378

3.0

5

s1p1, 11066.99, 1.037127, 1
s1p2, 11212.16, .6186247, 1
s1p3, 11132.94, 1.228176, 1
s1p4, 11057.7, 1.403529, 1
s1n1, 15541.27, 1.57503, 1
s1n2, 15791.17, .1862713, 1
s1n3, 15172.9, 1.418626, 1
s1n4, 15544.01, 2.052096, 1
s2p1, 11018.19, 1.071981, 1
s2p2, 11121.68, 1.587631, 1
s2p3, 11108.7, 1.835975, 1
s2p4, 10991.05, 1.579509, 1
s2n1, 15612.13, 1.966904, 1
s2n2, 15300.73, .4521432, 1

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```
'*******************************************************************
'Visual Basic Program Scan.bas
'*******************************************************************

'Declaration: Define Variables in Program++++++++++++++++++++++++++++++++++

Attribute VB_Name = "wireup"
Global v1 As Single
Global vo As Single
Global BRD As Integer
Global HP As Integer
Global HPD As Integer
Global HPT As Integer
Global HPI As Integer
Global SCN As Integer
Global EMI As Integer
Global nn As Integer
Global temp As Single
Global textout As String
Global dd1 As Double
Global dd2 As Double
Global rd As Double
Global ntry As Integer
Global nch As Integer
Global sb As Integer
Global ns As Integer
Global ii As Integer
Global nt As Integer
Global OVN As Integer
Global ov1 As Integer

'Subroutine GetTemp: Measure Temperature with Multimeter and
'Thermometer++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Sub GetTemp(temp)
Static PI, DD, A0, A1, A2, A3, T, A, B, c As Double
Static P, Q, R, TH1, TH2, TH3, T1, T2, T3 As Double
Static DUMMY As String * 16
nd = 10 'Number of Measurements to average
A0 = -11.61220418133
A1 = 5501.094308452
A2 = -192256.0980243
A3 = -1871564.641436
```

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```
PI = 4# * Atn(1)
DUM# = 0#
Call ibwrt(HPT, "*RST")
Call ibwrt(HPT, "*CLS")
Call ibwrt(HPT, "CONF:RES 1E8")
Call ibwrt(HPT, "TRIG:DEL:AUTO ON")
Call ibwrt(HPT, "SAMP:COUN 3")
Call ibwrt(HPT, "CALC:FUNC AVER")
Call ibwrt(HPT, "CALC:STAT ON")
Call ibwrt(HPT, "INIT")
Call ibwrt(HPT, "CALC:AVER:AVER?")
Call ibrd(HPT, DUMMY)
DUM# = Val(LTrim$(RTrim$(DUMMY)))
'Calculating the Oven Temperature corresponding to
'measured thermistor resistance. The following
'is the equation that the manufacturer (THERMOTRONICS)
'provided thermes = exp(A0 + A1/temp + A2/temp^2 +
'A3/temp^3
'** NOTE ** thermres is in kOhms and temp is in K
DUM# = DUM# / 1000 ' Thermres
T = A0 - Log(DUM#)
A = A1 / T
B = A2 / T
c = A3 / T
P = (3# * B - A ^ 2) / 3#
Q = (2 * A ^ 3 - 9# * A * B + 27# * c) / 27#
R = 2# * Sqr(-P / 3#)
DD = 3# * Q / (P * R)
TH1 = (Atn(-DD / Sqr(-DD * DD + 1)) + PI / 2#) / 3#
TH2 = TH1 + 2# * PI / 3#
TH3 = TH1 + 4# * PI / 3#
R1# = -A / 3# + R * Cos(TH1)
R2# = -A / 3# + R * Cos(TH2)
R3# = -A / 3# + R * Cos(TH3)
temp = R1#
End Sub

'Subroutine GetMeasurement: Measure Voltage of Power Supply 'with Multimeter,
'and Current with Electrometer.  'Resistance of sensors (v1) are then
'Obtained.++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Sub GetMeasurement(v1)
'SCPI Language
Static DUMMY As String * 18
```

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```
Static AMP As String * 18
DoEvents
Call ibwrt(HP, "SAMP:COUN 1")
Call ibwrt(HP, "read?")
Call ibrd(HP, DUMMY)
Call ibwrt(EMI, "F1R0C0Z0N0G1T0X")
Call ibrd(EMI, AMP)
v1 = Val(LTrim$(RTrim$(DUMMY))) / Val(LTrim$(RTrim$(AMP)))
'When measurement is doing for temperature dependent study,
'the following formula is used to save the time of measuring
'1.00727 is the voltage.  It need to be changed according to reading.
'v1 = 1.01192 / Val(LTrim$(RTrim$(AMP)))
Form1.Line1.BorderWidth = Int(10 * Rnd + 1)
End Sub

'Subroutine Initsetup: Initialize all the GPIB Controlled Equipment++++++++++++++++

Sub Initsetup(code1)
Rem Returns a zero when setup initalizes okay
'SCPI Language
Call ibfind("GPIB0", BRD) 'Find the GPIB board
Call ibfind("34401A-1", HP) 'Find the Diode meter
Call ibfind("34401A-3", HPT) 'Find thermistor meter
Call ibfind("ELECTRO", EMI) 'Find a electrometer
Call ibfind("SCAN7001", SCN) 'Find Keithley Scanner
Call ibfind("DELTA", OVN) 'Find Delta Design Oven
Call ibsic(BRD)
Call ibwrt(HP, "*RST; *CLS") 'Initialize
Call ibwrt(HPT, "*RST; *CLS") 'Initialize
Call ibwrt(EMI, "F1R0C0Z0N0G1T1X")
Call ibclr(SCN)
'Call ibclr(HP)
'HP 3478A Language
'   Call ibfind("GPIB1", BRD) 'FIND GBIP BOARD AND CHECK FOR ERRORS
'   Call ibfind("34401A-2", HP)  'FIND HP34401A (ME) METER AND CHECK FOR
ERRORS
'   Call ibfind("SCAN7001", SCN) 'FIND KEITHLEY 705 SCANNER with a MATRIX
CARD
'Call ibsic(BRD)        'CLEAR BOARD
'Call ibclr(HP)         'CLEAR HP METER "HPME"
'Call ibclr(SCN)        'CLEAR SCANNER
'Call ibwrt(HP, "F1R1")  'RESET HP METER FOR 30 DC VOLTS RANGE
'MEASUREMENT
```

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```
'Call ibwrt(HP, "F3R5")   'RESET HP METER FOR 30 K Ohms RANGE
'MEASUREMENT
code1 = 0
End Sub

'Subroutine Chipid: Measure Chip ID+++++++++++++++++++++++++++++++++++

Sub Chipid()
Open "c:\temp\check.dat" For Output As #5
nn = 0
For i = 1 To 9
cc$ = ":clos (@1!" + Str$(10 + i) + ")"
        Call ibwrt(SCN, cc$)
        Call Getid(v1)
        textout = textout + Str$(v1) + Chr(13) + Chr(10)
        If v1 >= 300# Then
        ni = 1
        Else
        ni = 0
        End If
        nn = nn + ni * 2 ^ (i - 1)
    op$ = ":open (@1!" + Str$(10 + i) + ")"
    Call ibwrt(SCN, op$)
    Print #5, Str$(10 + i)
 Next i
 id$ = "chid" + "," + LTrim$(Str(nn)) + Chr(13) + Chr(10)
    textout = textout + id$ + Chr(13) + Chr(10)
    Form1.DisText.Text = textout
 End Sub

'Subroutine Std: Calculate Standard Deviation of Measured Resistance of
'Sensors+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Sub Std(v1, ov1)
nc = Int(Val(Form1.text4.Text))
prd = Val(LTrim$(RTrim$(Form1.text6.Text)))
ntry = 0
Do
ntry = ntry + 1
dd1 = 0
dd2 = 0
For im = 1 To nc
If ov1 = 1 Then
Call getmeasurOV(v1)
```

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```
GoTo 20
End If
If ov1 = 0 Then
Call GetMeasurement(v1)
End If
20
   Form1.TempText.Text = vo
   Form1.ResText.Text = v1
   DoEvents
vo = v1
If Abs(v1) >= 50000# Then GoTo 50
dd1 = dd1 + v1 * v1 / (nc - 1)
dd2 = dd2 + v1
Next im
Form1.text3.Text = ntry: Form1.text4.Text = nc
rd = Sqr(Abs(dd1 - dd2 * dd2 / (nc * (nc - 1))))
Form1.text2.Text = rd
If ntry >= 3 Then
Exit Do
End If
Loop Until rd <= prd
v1 = dd2 / nc
50
End Sub

'Subroutine Site: Control Channel Switch of Scanner.  The Board#, Site#, Resistor#, and
'Channel# are Defined in Form Code.+++++++++++++++++++++++++++++++++++++

Sub Site(ov1, temp, ii, ns, nt, nch)
Dim c(2) As Integer
'Open "c:\temp\check.dat" For Output As #5
Call ibwrt(SCN, ":open all")
vo = 0#
'ii=Board #
'ns=Site #
'nt=Resistor type #
'nch=Chanel #
'P1 (0 deg)
   res$ = "s" + LTrim$(Str(ns)) + "p1"
   Form1.R1Text.Text = res$
   If nt = 2 Then
      c(1) = 3 + 10 * (nch - 1): c(2) = 1 + 10 * (nch - 1)
   Else
      c(1) = 2 + 10 * (nch - 1): c(2) = 4 + 10 * (nch - 1)
```

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```
    End If
    For i = 1 To 2
          cc$ = ":clos (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
       Call ibwrt(SCN, cc$)
    Next i
start = Timer: Do: finish = Timer: Loop Until (finish - start) >= 0.05
Call std(v1, ov1)
'Set up OUTPUT Display
   'textout = textout + Str(nch) + "," + Str(v1) + Chr(13) + Chr(10)
   textout = textout + res$ + "," + Str(v1) + "," + Str(rd) + "," + Str(ntry) + Chr(13) +
Chr(10)
   Form1.DisText.Text = textout
   For i = 1 To 2
         op$ = ":open (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
   Call ibwrt(SCN, op$)
   Next i
   'Call GetTemp(temp)
   'Form1.Text1.Text = Str(temp - 273.15)
   Form1.Text1.Text = Str(ov1)
Print #5, res$; ","; temp - 273.5; ","; v1; ","; rd; ", "; ntry
'P2 (90 deg)
      res$ = "s" + LTrim$(Str(ns)) + "p2"
   Form1.R1Text.Text = res$
   If nt = 2 Then
      c(1) = 2 + 10 * (nch - 1): c(2) = 4 + 10 * (nch - 1)
   Else
      c(1) = 1 + 10 * (nch - 1): c(2) = 3 + 10 * (nch - 1)
   End If
   For i = 1 To 2
         cc$ = ":clos (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
      Call ibwrt(SCN, cc$)
   Next i
start = Timer: Do: finish = Timer: Loop Until (finish - start) >= 0.05
Call std(v1, ov1)
'Set up OUTPUT Display
   'textout = textout + Str(nch) + "," + Str(v1) + Chr(13) + Chr(10)
   textout = textout + res$ + "," + Str(v1) + "," + Str(rd) + "," + Str(ntry) + Chr(13) +
Chr(10)
   Form1.DisText.Text = textout
   For i = 1 To 2
         op$ = ":open (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
   Call ibwrt(SCN, op$)
   Next i
   'Call GetTemp(temp)
```

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```
    'Form1.Text1.Text = Str(temp - 273.15)
 Print #5, res$; ","; temp - 273.5; ","; v1; ","; rd; ", "; ntry
 'P3 (+45 deg)
     res$ = "s" + LTrim$(Str(ns)) + "p3"
    Form1.R1Text.Text = res$
  If nt = 2 Then
      c(1) = 1 + 10 * (nch - 1): c(2) = 10 + 10 * (nch - 1)
    Else
      c(1) = 9 + 10 * (nch - 1): c(2) = 4 + 10 * (nch - 1)
    End If
    For i = 1 To 2
        cc$ = ":clos (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
      Call ibwrt(SCN, cc$)
    Next i
start = Timer: Do: finish = Timer: Loop Until (finish - start) >= 0.05
Call std(v1, ov1)
'Set up OUTPUT Display
   'textout = textout + Str(nch) + "," + Str(v1) + Chr(13) + Chr(10)
   textout = textout + res$ + "," + Str(v1) + "," + Str(rd) + "," + Str(ntry) + Chr(13) +
Chr(10)
   Form1.DisText.Text = textout
   For i = 1 To 2
        op$ = ":open (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
   Call ibwrt(SCN, op$)
   Next i
   'Call GetTemp(temp)
   'Form1.Text1.Text = Str(temp - 273.15)
Print #5, res$; ","; temp - 273.5; ","; v1; ","; rd; ", "; ntry
'P4 (-45 deg)
    res$ = "s" + LTrim$(Str(ns)) + "p4"
   Form1.R1Text.Text = res$
  If nt = 2 Then
     c(1) = 9 + 10 * (nch - 1): c(2) = 4 + 10 * (nch - 1)
   Else
     c(1) = 1 + 10 * (nch - 1): c(2) = 10 + 10 * (nch - 1)
   End If
   For i = 1 To 2
        cc$ = ":clos (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
     Call ibwrt(SCN, cc$)
   Next i
start = Timer: Do: finish = Timer: Loop Until (finish - start) >= 0.05
Call std(v1, ov1)
'Set up OUTPUT Display
   'textout = textout + Str(nch) + "," + Str(v1) + Chr(13) + Chr(10)
```

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```
    textout = textout + res$ + "," + Str(v1) + "," + Str(rd) + "," + Str(ntry) + Chr(13) +
Chr(10)
    Form1.DisText.Text = textout
    For i = 1 To 2
        op$ = ":open (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
    Call ibwrt(SCN, op$)
    Next i
    'Call GetTemp(temp)
    'Form1.Text1.Text = Str(temp - 273.15)
Print #5, res$; ","; temp - 273.5; ","; v1; ","; rd; ", "; ntry
'N1 (0 deg)
        res$ = "s" + LTrim$(Str(ns)) + "n1"
    Form1.R1Text.Text = res$
    If nt = 2 Then
        c(1) = 5 + 10 * (nch - 1): c(2) = 4 + 10 * (nch - 1)
    Else
        c(1) = 1 + 10 * (nch - 1): c(2) = 6 + 10 * (nch - 1)
    End If
    For i = 1 To 2
        cc$ = ":clos (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
        Call ibwrt(SCN, cc$)
    Next i
start = Timer: Do: finish = Timer: Loop Until (finish - start) >= 0.05
Call std(v1, ov1)
'Set up OUTPUT Display
    'textout = textout + Str(nch) + "," + Str(v1) + Chr(13) + Chr(10)
    textout = textout + res$ + "," + Str(v1) + "," + Str(rd) + "," + Str(ntry) + Chr(13) +
Chr(10)
    Form1.DisText.Text = textout
    For i = 1 To 2
        op$ = ":open (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
    Call ibwrt(SCN, op$)
    Next i
    'Call GetTemp(temp)
    'Form1.Text1.Text = Str(temp - 273.15)
Print #5, res$; ","; temp - 273.5; ","; v1; ","; rd; ", "; ntry
'N2 (90 deg)
    res$ = "s" + LTrim$(Str(ns)) + "n2"
    Form1.R1Text.Text = res$
  If nt = 2 Then
      c(1) = 1 + 10 * (nch - 1): c(2) = 6 + 10 * (nch - 1)
    Else
      c(1) = 5 + 10 * (nch - 1): c(2) = 4 + 10 * (nch - 1)
    End If
```

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```
    For i = 1 To 2
         cc$ = ":clos (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
       Call ibwrt(SCN, cc$)
    Next i
 start = Timer: Do: finish = Timer: Loop Until (finish - start) >= 0.05
 Call std(v1, ov1)
 'Set up OUTPUT Display
    'textout = textout + Str(nch) + "," + Str(v1) + Chr(13) + Chr(10)
    textout = textout + res$ + "," + Str(v1) + "," + Str(rd) + "," + Str(ntry) + Chr(13) +
Chr(10)
    Form1.DisText.Text = textout
    For i = 1 To 2
         op$ = ":open (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
    Call ibwrt(SCN, op$)
    Next i
    'Call GetTemp(temp)
    'Form1.Text1.Text = Str(temp - 273.15)
Print #5, res$; ","; temp - 273.5; ","; v1; ","; rd; ", "; ntry
'N3 (+45 deg)
    res$ = "s" + LTrim$(Str(ns)) + "n3"
    Form1.R1Text.Text = res$
    If nt = 2 Then
       c(1) = 7 + 10 * (nch - 1): c(2) = 4 + 10 * (nch - 1)
    Else
       c(1) = 1 + 10 * (nch - 1): c(2) = 8 + 10 * (nch - 1)
    End If
    For i = 1 To 2
         cc$ = ":clos (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
       Call ibwrt(SCN, cc$)
    Next i
start = Timer: Do: finish = Timer: Loop Until (finish - start) >= 0.05
Call std(v1, ov1)
'Set up OUTPUT Display
    'textout = textout + Str(nch) + "," + Str(v1) + Chr(13) + Chr(10)
    textout = textout + res$ + "," + Str(v1) + "," + Str(rd) + "," + Str(ntry) + Chr(13) +
Chr(10)
    Form1.DisText.Text = textout
    For i = 1 To 2
         op$ = ":open (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
    Call ibwrt(SCN, op$)
    Next i
    'Call GetTemp(temp)
    'Form1.Text1.Text = Str(temp - 273.15)
Print #5, res$; ","; temp - 273.5; ","; v1; ","; rd; ", "; ntry
```

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```
'N4 (-45 deg)
    res$ = "s" + LTrim$(Str(ns)) + "n4"
    Form1.R1Text.Text = res$
  If nt = 2 Then
      c(1) = 1 + 10 * (nch - 1): c(2) = 8 + 10 * (nch - 1)
    Else
      c(1) = 7 + 10 * (nch - 1): c(2) = 4 + 10 * (nch - 1)
    End If
    For i = 1 To 2
        cc$ = ":clos (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
      Call ibwrt(SCN, cc$)
    Next i
start = Timer: Do: finish = Timer: Loop Until (finish - start) >= 0.05
Call std(v1, ov1)
'Set up OUTPUT Display
   'textout = textout + Str(nch) + "," + Str(v1) + Chr(13) + Chr(10)
   textout = textout + res$ + "," + Str(v1) + "," + Str(rd) + "," + Str(ntry) + Chr(13) +
Chr(10)
   Form1.DisText.Text = textout
   For i = 1 To 2
        op$ = ":open (@" + LTrim(RTrim$(Str$(ii))) + "!" + Str$(c(i)) + ")"
   Call ibwrt(SCN, op$)
   Next i
   'Call GetTemp(temp)
   'Form1.Text1.Text = Str(temp - 273.15)
Print #5, res$; ","; temp - 273.5; ","; v1; ","; rd; ", "; ntry
End Sub

'Subroutine Getid: Obtain the Resistance of Burned or Non-Burned Fuse for the
'Calculation in Subroutine Chipid.++++++++++++++++++++++++++++++++++++++

Sub Getid(v1)
'SCPI Language
Static DUMMY As String * 18
Static AMP As String * 18
DoEvents
Call ibwrt(HP, "*RST; *CLS")
Call ibwrt(HP, "CONF:RES")
Call ibwrt(HP, "TRIG:DEL:AUTO ON")
Call ibwrt(HP, "SAMP:COUN 1")
Call ibwrt(HP, "CALC:FUNC AVER")
Call ibwrt(HP, "CALC:STAT ON")
Call ibwrt(HP, "INIT")
Call ibwrt(HP, "CALC:AVER:AVER?")
```

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```
Call ibrd(HP, DUMMY)
v1 = Val(LTrim$(RTrim$(DUMMY)))
Form1.Line1.BorderWidth = Int(10 * Rnd + 1)
End Sub

'Subroutine SetTemp: Set a Desired Temperature (Tempin) Defined in Form Code.
'++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Sub SetTemp(Tempin As Single)
Static tmp As String
Static ActTemp As Single
Static LasTemp As Single
Static flag1 As Integer
Static dif As Single
'Set Oven
'tmp = "+" + Format$(Tempin, "000.0") + "T"
tmp = Format$(Tempin, "000.0")
Form1.Text1.Text = LTrim$(RTrim$(tmp))
'Call ibwrt(OVN, LTrim$(RTrim$(tmp)))
Call ibwrt(OVN, "setpoint" + Str$(tmp))
Call ibwrt(OVN, "setpoint?")
LasTemp = 0
flag1 = 0
Do
   DoEvents
   Call GetTemp(ActTemp)
  Form1.Text1.Text = Str(ActTemp)
   dif = ActTemp - LasTemp
   If Abs(dif) < 0.3 Then
   flag1 = flag1 + 1
   Else
      flag1 = 0
   End If
   start = Timer
   'Do: DoEvents: finish = Timer: Loop Until (finish - start) > 5
   Do: DoEvents: finish = Timer: Loop Until (finish - start) > 80
   LasTemp = ActTemp
Loop Until flag1 = 1
End Sub

'Subroutine GetMeasureOV: Similar to Subroutine GetMeasurement (v1).  When
'Measurement Is Done as A Function of Temperature, Especially for Quickly Changing
'Temperature, A fixed Voltage Is Used to Reduce Measurement Time.
'++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
```

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```
Sub GetMeasurOV(v1)
'SCPI Language
Static DUMMY As String * 18
Static AMP As String * 18
DoEvents
Call ibwrt(EMI, "F1R0C0Z0N0G1T1X")
Call ibrd(EMI, AMP)
'When measurement is doing for temperature dependent study,
'the following formula is used to save the time of measuring
'1.00727 is the voltage.  It need to be changed according to reading.
v1 = 1.01194 / Val(LTrim$(RTrim$(AMP)))
'v1 = Val(LTrim$(RTrim$(DUMMY)))
End Sub
```

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```
**********************************************************************
'Form Code: Define Commands, TextBox, Label etc. in the Main Form.
'The Properties of Each Object are not Listed
**********************************************************************

VERSION 4.00
Begin VB.Form Form1
  Caption        =  "BMW Test Chip"
BeginProperty Font
    name           =  "MS Sans Serif"
EndProperty
LinkTopic      =  "Form1"
Begin VB.CommandButton Cure
    Caption        =  "Cure"
End
Begin VB.CommandButton Command4
    Caption        =  "Oven L-H"
  End
 Begin VB.CommandButton Command3
    Caption        =  "Chip ID"
End
 Begin VB.CommandButton Command2
    Caption        =  "Reset"
End
Begin VB.CommandButton Command1
    Caption        =  "Save"
End
  Begin VB.TextBox DisText
End
  Begin VB.CommandButton ExitCommand
Caption        =  "Exit"
End
Begin VB.TextBox ResText
End
 Begin VB.TextBox TempText
End
 Begin VB.CommandButton StartCommand
Caption        =  "Measure"
End
  Begin VB.PictureBox Panel3D1
Begin VB.TextBox Text6
Text           =  "100.0"
End
Begin VB.TextBox Text4
```

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```
Text          =  "2"
End
Begin VB.TextBox Text3
End
Begin VB.TextBox Text2
End
Begin VB.TextBox Text1
End
Begin VB.TextBox R1Text
End
Begin VB.Label Label11
        Caption        =  "Ohms"
End
 Begin VB.Label Label10
        Caption        =  "Max.Std Dev"
End
Begin VB.Line Line1
End
 Begin VB.Label Label7
        Caption        =  "New reading"
End
 Begin VB.Label Label3
        Caption        =  "Old reading"
End
Begin VB.Label Label6
        Caption        =  "#of data"
End
Begin VB.Label Label5
        Caption        =  "#of Try"
End
Begin VB.Label Label4
        Caption        =  "Std Dev"
End
Begin VB.Label Label1
        Caption        =  "Current Temp"
End
  End
Begin VB.Label TitleLabel
name          =  "MS Sans Serif"
EndProperty
End
Begin VB.Label Statuslabel2
End
```

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```
Begin VB.Label Statuslabel1
Caption         =   "Setup Status:"
End
End
Attribute VB_Name = "Form1"
Attribute VB_Creatable = False
Attribute VB_Exposed = False

Private Sub Command1_Click()
SaveForm.Show 1
End Sub

Private Sub Command2_Click()
Unload Form1
Form1.Show 1
End Sub

Private Sub Command3_Click()
'Put the output lines on voltage Multimeter
Call chipid
End Sub

'Subroutine Oven: Measure Sensor Resistance as a Function of Temperature.
'++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Private Sub Oven_Click()
'Need to Change the Voltage in "GetmeasurOV" Subroutine.
'Change the Average Data Number to Be 2 to Save the Measurement Time.
'Set Suitable Time (Finish-Start) in "SetTemp" Subroutine.
'The Actual Oven Temperature May Be About 7 Degree C Higher than Oven Shows.
'Check Thermal Cycle: tbegin, tfinish, tincrement.
'If the Temperature Goes Up, tincrement Should Be Positive, and the
'Conditions Which Is Used to Judge the End Need to Be Checked.
'When the Temperature Goes up, It Should Be "curtemp! >= tfinish"
'and "Loop Until curtemp! > tfinish"
ExitCommand.Enabled = True
StartCommand.Enabled = False
Call GetTemp(temp)
Form1.Text1.Text = Str(temp - 273.15)
Open "c:\temp\sav.dat" For Output As #5
'Open "c:\temp\res.dat" For Output As #1
ov1 = 1
Call ibwrt(OVN, "version?")
Call ibwrt(OVN, "highset 200.0")
```

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```
 Call ibwrt(OVN, "highset?")
 Call ibwrt(OVN, "lowset -100.0")
 Call ibwrt(OVN, "lowset?")
 Call ibwrt(OVN, "heat on")
 Call ibwrt(OVN, "cool on")
 'set #1 step
 tbegin = -30#
 tfinish = 150#
 tincrement = 10#
 'Measurement loop
 curtemp! = tbegin
 flag1 = 0
 j% = 0
 Do
    'Setting oven
    Call SetTemp(curtemp!)
    Form1.Text1.Text = Str(temp - 273.15)
  Call GetTemp(realtemp!)
 textout = Str(realtemp! - 273.15) + "," + Chr(13) + Chr(10)
 Form1.DisText.Text = textout
 temp = realtemp!

 'Define Site#, Board#, Channel#, and Resistance Type.  Same Program will Be Used in
 'Following "Cure" and "Start" Subroutines.++++++++++++++++++++++++++++++++

 'site #1
 1
 ii = 1
 ns = 1
 nt = 1
 nch = 2
 Call Site(ov1, temp, ii, ns, nt, nch)
 'site #2
 2
 ii = 1
 ns = 2
 nt = 1
 nch = 3
 Call Site(ov1, temp, ii, ns, nt, nch)
 'site #12
 12
 ii = 1
 ns = 12
 nt = 2
```

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```
nch = 1
'Call Site(ov1, temp, ii, ns, nt, nch)
'Site #4
4
ii = 2
ns = 4
nt = 2
nch = 1
'Call Site(ov1, temp, ii, ns, nt, nch)
'Site #3
3
ii = 1
ns = 3
nt = 1
nch = 4
'Call Site(ov1, temp, ii, ns, nt, nch)
'Site #5
5
ii = 2
ns = 5
nt = 2
nch = 2
Call Site(ov1, temp, ii, ns, nt, nch)
'Site #9
9
ii = 3
ns = 9
nt = 2
nch = 2
'Call Site(ov1, temp, ii, ns, nt, nch)
'site #7
7
ii = 2
ns = 7
nt = 1
nch = 4
Call Site(ov1, temp, ii, ns, nt, nch)
'Site #6
6
ii = 2
ns = 6
nt = 2
nch = 3
Call Site(ov1, temp, ii, ns, nt, nch)
```

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```
'Site #11
11
ii = 3
ns = 11
nt = 2
nch = 4
'Call Site(ov1, temp, ii, ns, nt, nch)
'Site #10
10
ii = 3
ns = 10
nt = 2
nch = 3
Call Site(ov1, temp, ii, ns, nt, nch)
'Site #8
8
ii = 3
ns = 8
nt = 1
nch = 1
Call Site(ov1, temp, ii, ns, nt, nch)
'End of Definition. +++++++++++++++++++++++++++++++++++++++++++++
 'Setting next temperature
   j% = j% + 1
   curtemp! = tbegin + j% * tincrement
   If curtemp! >= tfinish And flag1 = 0 Then
      curtemp! = tfinish
      flag1 = 1
   End If
   DoEvents
Loop Until curtemp! > tfinish
Close #5
StartCommand.Enabled = True
'Bring the temp back down
curtemp! = 20!
Call SetTemp(curtemp!)
Call ibwrt(OVN, "heat off")
Call ibwrt(OVN, "cool off")
End Sub

'Subroutine Cure: Get the Resistance Measurements during Encapsulant Curing Cycle.
'+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Private Sub Cure_Click()
```

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```
ExitCommand.Enabled = True
StartCommand.Enabled = False
Call GetTemp(temp)
Form1.Text1.Text = Str(temp - 273.15)
Open "c:\temp\sav.dat" For Output As #5
'Open "c:\temp\res.dat" For Output As #1
'Measurement loop
j% = 0
timeincre# = 1
Time# = 0
start1 = Timer
Do
   DoEvents
Time# = Timer
textout = Str(Time# - start1) + Chr(13) + Chr(10)
   Form1.DisText.Text = textout
Print #5, Time# - start1
Call GetTemp(temp)
Print #5, temp - 273.5
ov1 = 1

'Insert the Previous Definition Program for Board #, Site #, Resistance Type #, and
'Channel # ==============================================

Time# = Timer
textout = textout + Str(Time# - start1) + Chr(13) + Chr(10)
   Form1.DisText.Text = textout
'Print #5, Time# - start1
start = Timer
   Do: DoEvents: finish = Timer: Loop Until (finish - start) > timeincre#
    j% = j% +
Loop Until j% = 3
Close #5
Cure.Enabled = True
End Sub

Private Sub Command5_Click()
End Sub

Private Sub ExitCommand_Click()
Form1.Hide
Unload Form1
End
End Sub
```

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```
Private Sub Form_Load()
'ChDrive "c:"
'ChDir "\'yidazou\vb"
Call initsetup(code1)
If code1 = 0 Then
   Statuslabel2.ForeColor = &HFF00&
   Statuslabel2.Caption = "OKAY"
   StartCommand.Enabled = True
ElseIf code1 = 1 Then
   Statuslabel2.ForeColor = &HFF&
   Statuslabel2.Caption = "ERROR"
End If
'textout = "Resistor #,  Resistance, StdDev, # Try" + Chr(13) + Chr(10)
Form1.DisText.Text = textout
End Sub

'Subroutine Start: Measure Resistance after Encapsulation at Room Temperature
'++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Private Sub StartCommand_Click()
ExitCommand.Enabled = True
StartCommand.Enabled = False
Call GetTemp(temp)
Form1.Text1.Text = Str(temp - 273.15)
Open "c:\temp\sav.dat" For Output As #5
'Open "c:\temp\res.dat" For Output As #1
'GoTo 11
ov1 = 0

'Insert the Previous Definition Program for Board #, Site #, Resistance Type #, and
'Channel # =================================================

Close #5
'Close #1
StartCommand.Enabled = True
End Sub

Private Sub Text1_Click()
Call GetTemp(temp)
Form1.Text1.Text = Str(temp - 273.15)
End Sub
```

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APPENDIX B

WIRING DIAGRAMS FOR AAA2, BMW-1 AND BMW-2 SENSOR MEASUREMENTS

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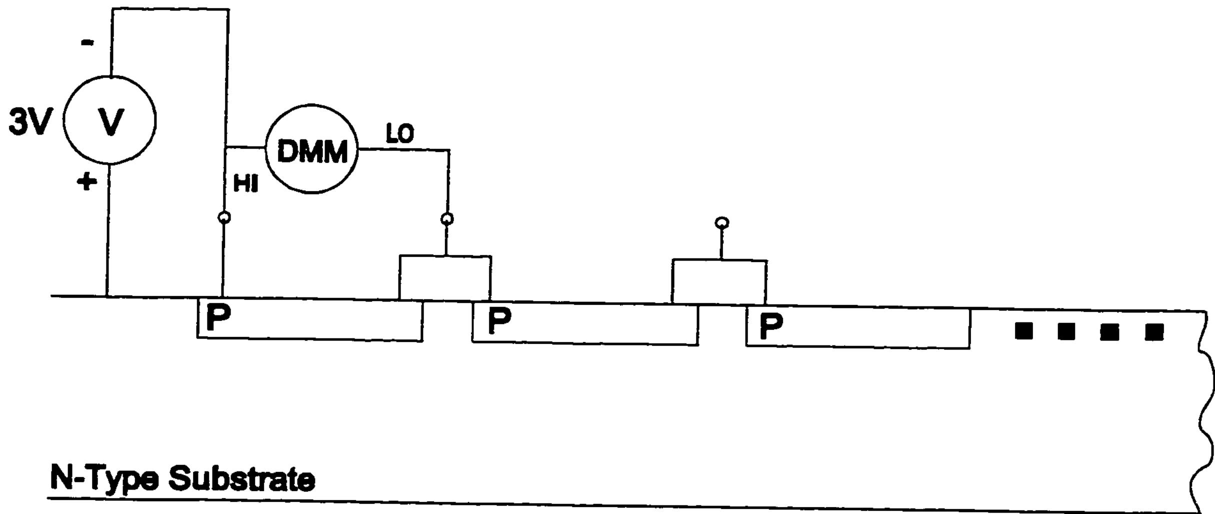
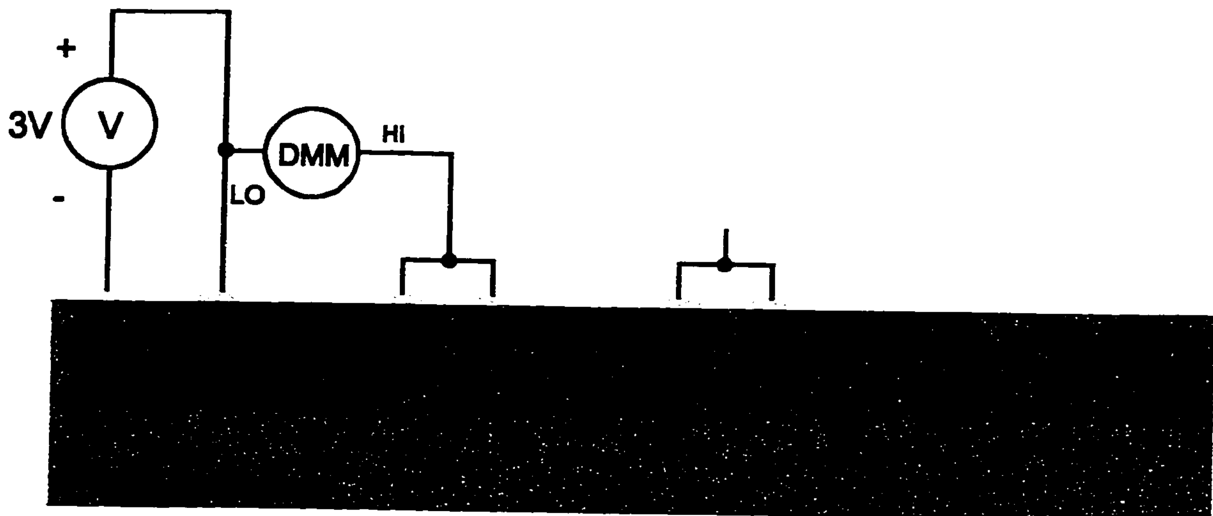
AAA2: P-Type Resistors Bias Setup (HP meters, Manual)



AAA2: N-Type Resistors Bias Setup (HP meters, Manual)



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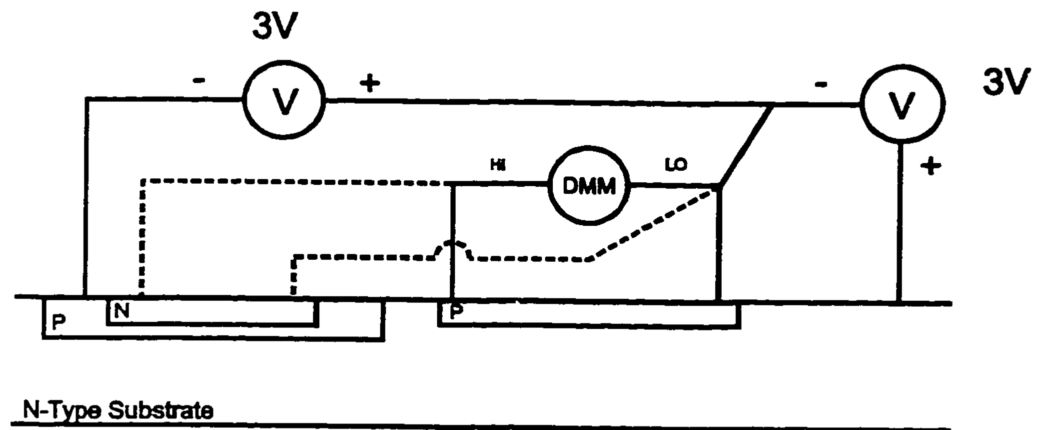
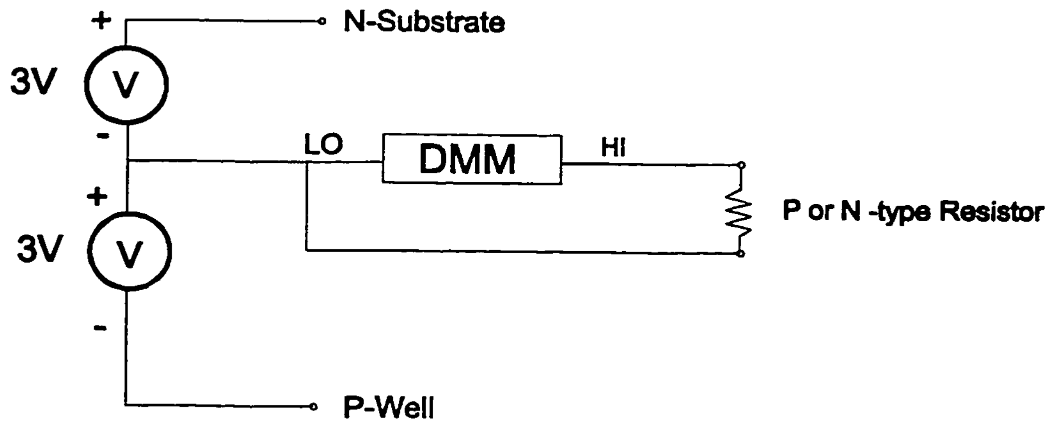
AAA2: P&N - Type Resistor Measurement Setup





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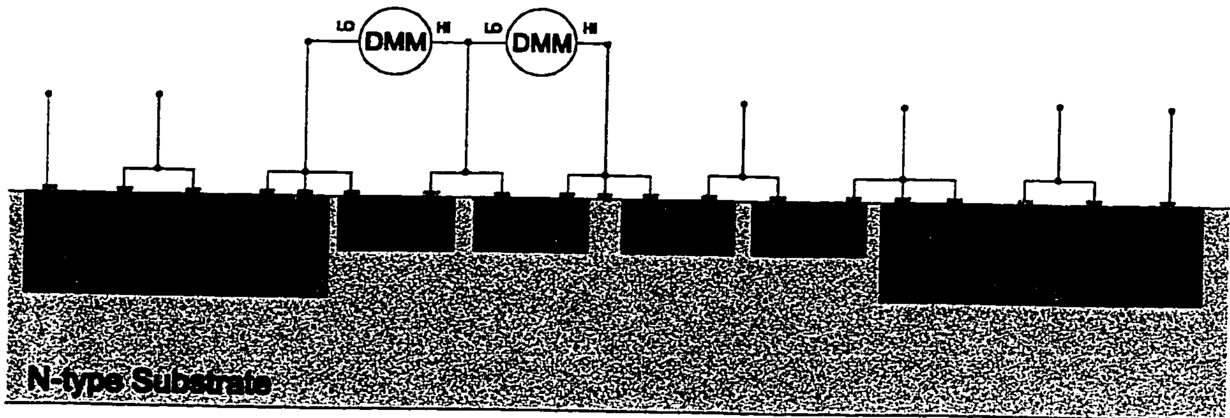

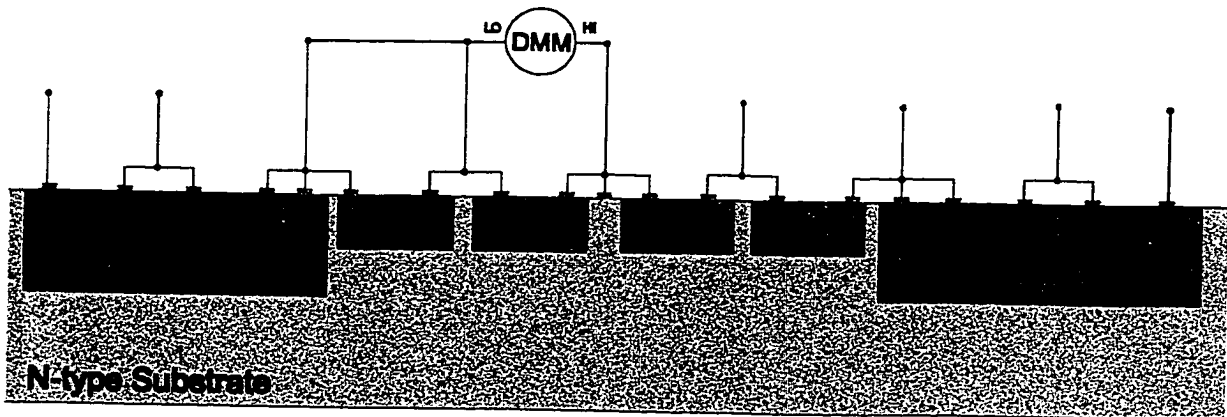

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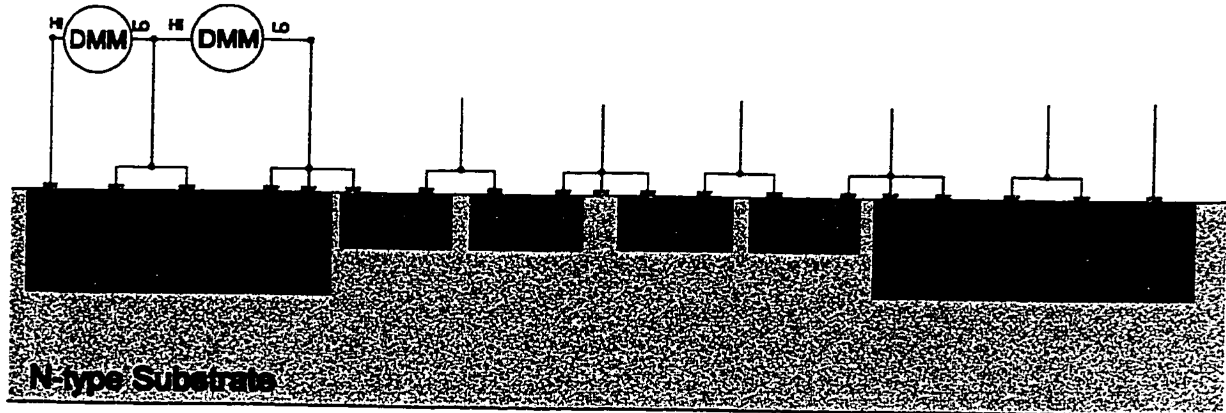
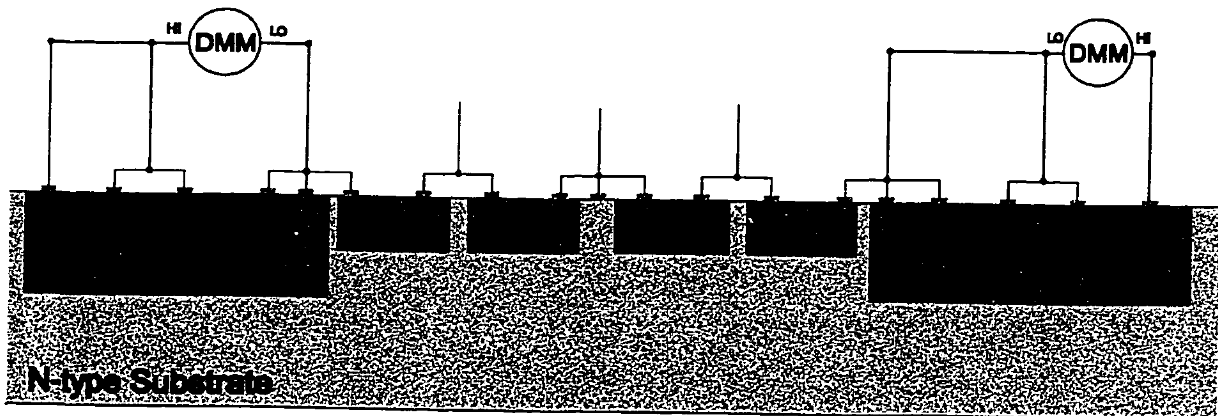
BMW-1: N-Type Resistors
Bias Setup #1
HP Meters



BMW-1: N-Type Resistors
Bias Setup #2
HP Meters



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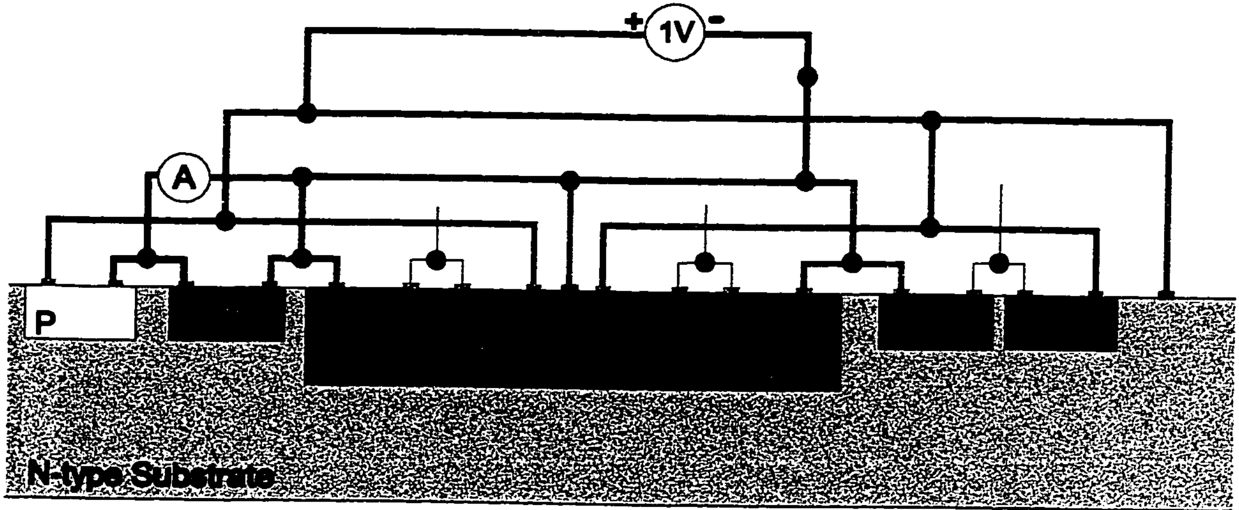
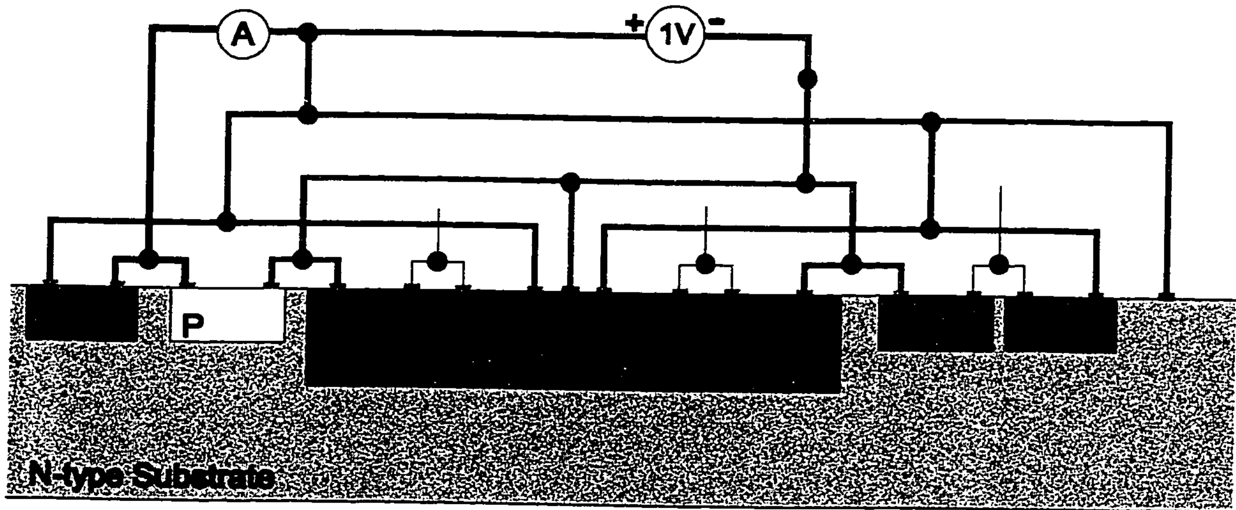
BMW-2: P-Type Resistors
Resistance Measurement (Biased)
HP Meters



BMW-2: P-Type Resistors
Resistance Measurement (Biased)
HP Meters



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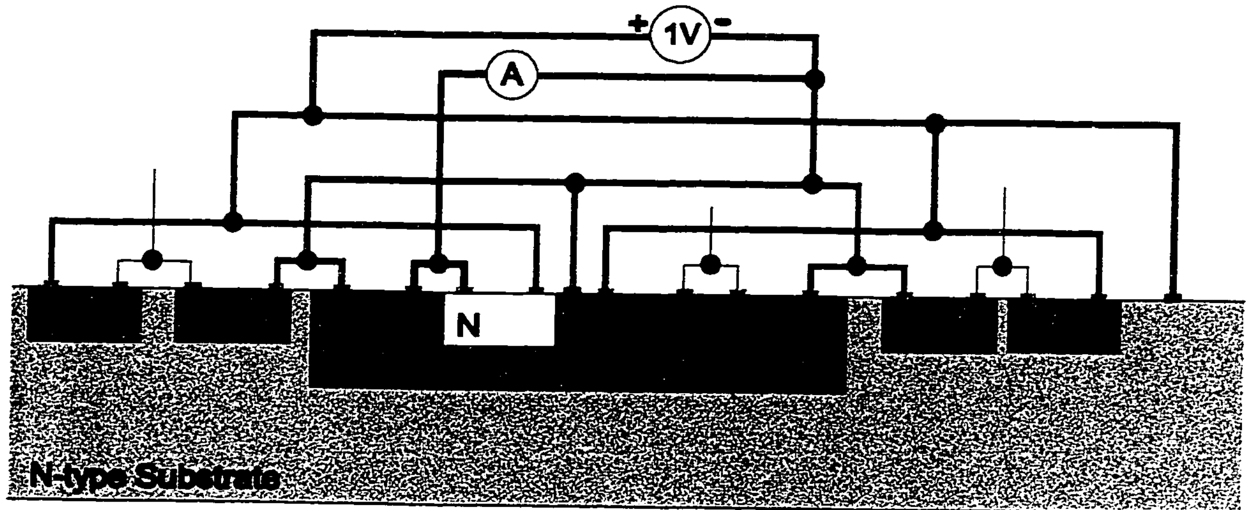
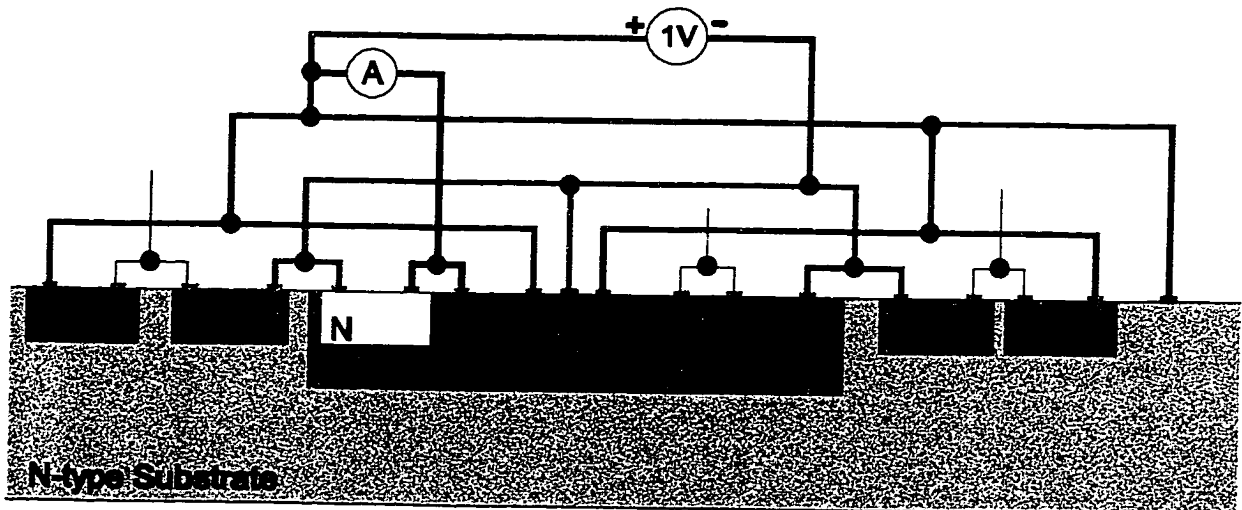
BMW-2: N-Type Resistors
Resistance Measurement (Biased)
HP Meters



BMW-2: N-Type Resistors
Resistance Measurement (Biased)
HP Meters



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